Microprocessors Laboratory

A/D Programming

LISHA/UFSC

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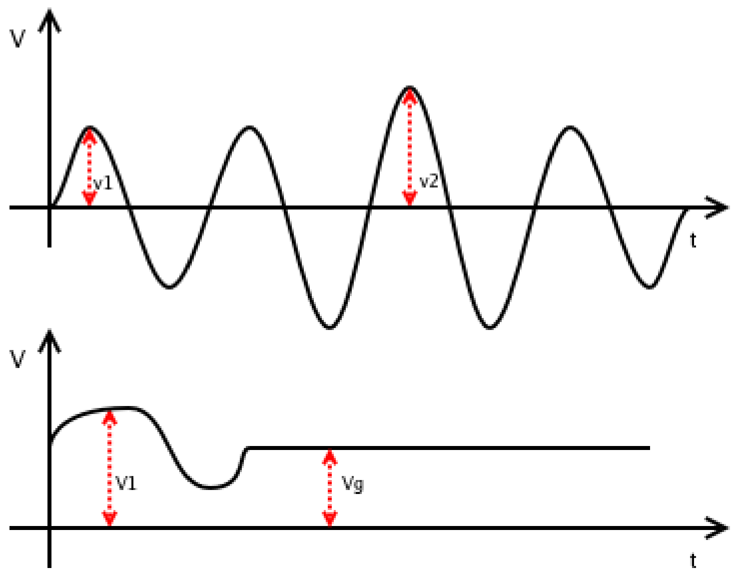
Signals

- Signal
  - Detectable transmitted energy that can be used to carry information
- Analog signals
  - Continuous nature
  - May take any value within a range
  - Information carried in (variations of) amplitude, frequency, or phase



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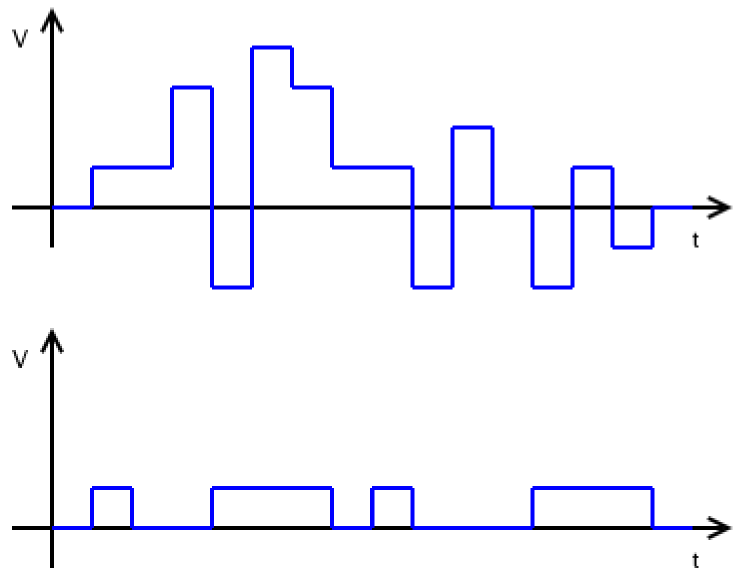
Signals

- Digital signals
  - Discrete nature
  - Finite number of possible states within a range
  - Information carried in discrete signal states



Signals: Computers and the Real World

- The world is analog by nature
- Digital computers are... well, digital (and usually binary)!
- Interfacing analog signals to digital processors or microcontrollers is inevitable
  - Digital music and video
  - Digital telephony
  - Sensors and actuators

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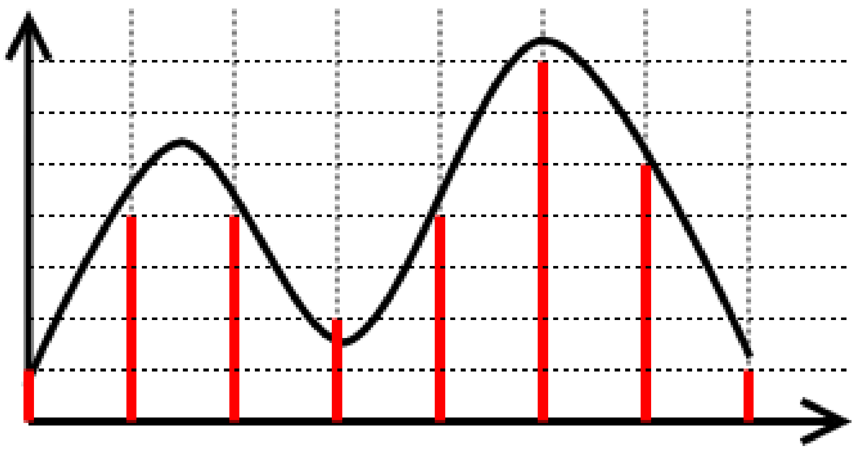
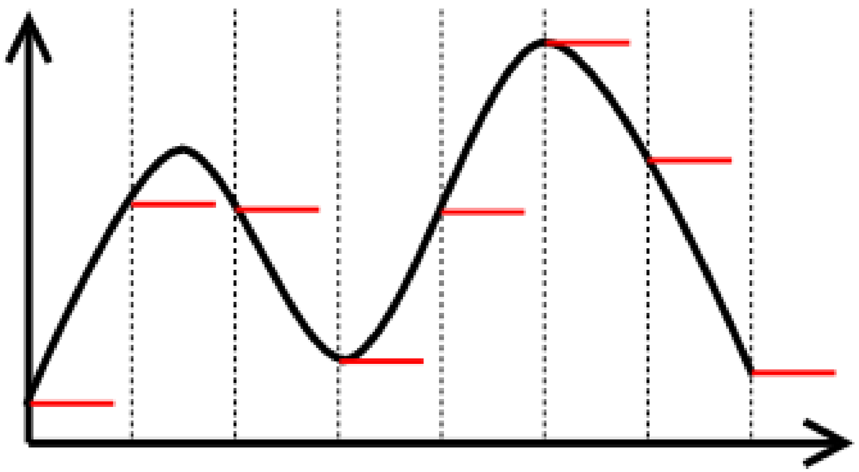
Analog to Digital Conversion

- The analog signal is sampled (i.e. measured) at a regular interval and each sample is quantized (i.e. converted to discrete numeric values) by a given value that approximates to the analog value.



Sampling

- The analog signal is measured periodically
- Sampling rate
  - Number of samples that are taken on a time period (e.g. a second)

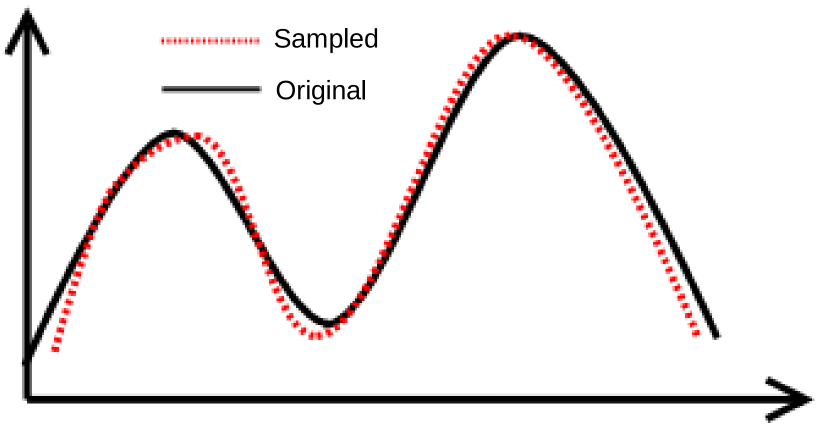


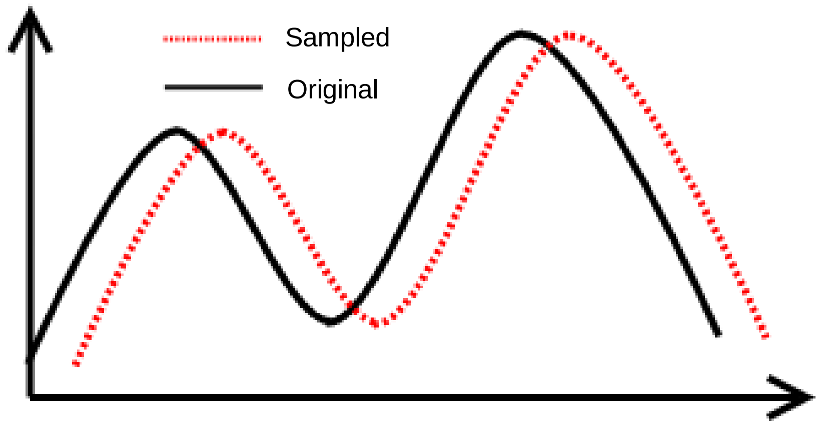
Sampling

- Nyquist's theorem
  - “The sampling frequency must be greater than twice the highest frequency of the input signal in order to be able to reconstruct the original perfectly from the sampled version”
  - f Hz analog signal => 2 x f Hz sampling rate
  - Example: Hi-Fi audio
    - 20-20000 Hz signal => 40 kHz sampling frequency
- The sampling rate determines the speed of the conversion device
  - Fast devices cost more

Irregular Sampling

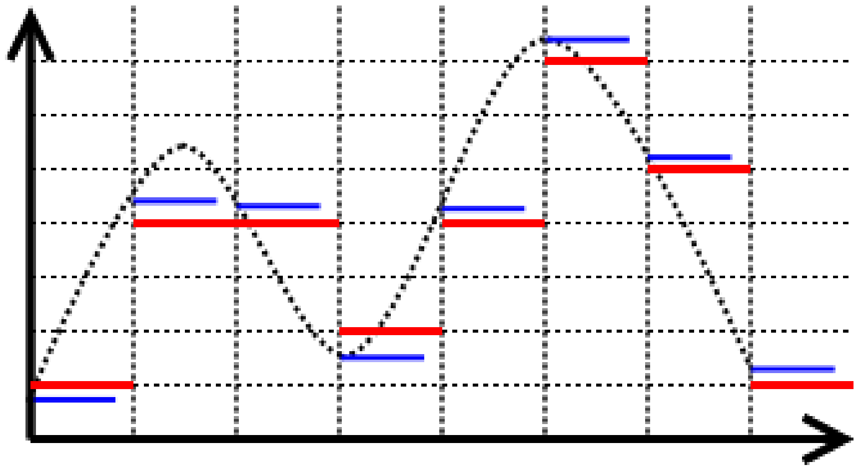
- Sampling must be performed on a regular basis with exactly the same time between samples
  - Irregular sampling leads to conversion errors
    - Early or late sampling, jitter, delayed sampling





Quantization

- The sampled signal is quantized (converted to discrete numeric values)
- The number of quantization steps determine how many discrete values a given sample may take



Quantization

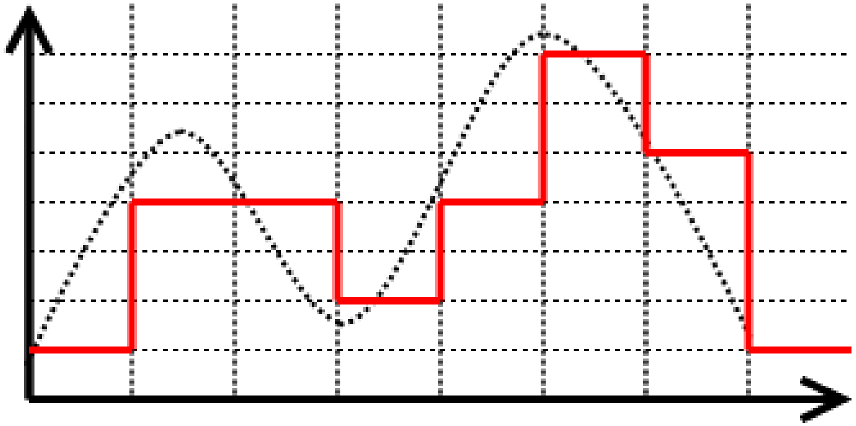
- The size of the quantization step determines the resolution of the conversion
  - Dependent on the number of bits used to represent the analog value and the analog signal's amplitude
- Example (analog signal range 0-1):

Size	Resolution (Size of each quantization step)
4 bit	0.06250000
8 bit	0.00390625
16 bit	0.00001525

- Higher resolution means more precise conversions
  - High resolution devices cost more

Codification

- A digital value is associated with each quantized sample
- The maximum error in codification for a "perfect ADC" is +/- 1/2 LSB, where LSB is the size in volts of each quantization step

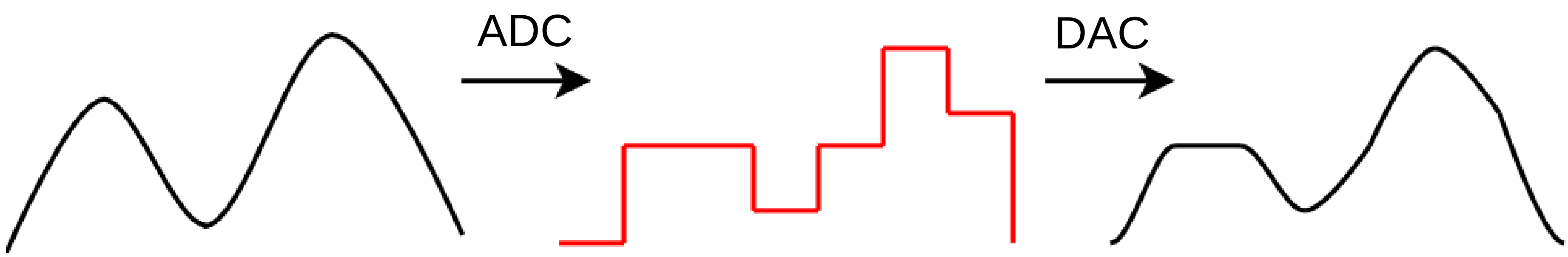


Digital Representation of Signals

- PCM (Pulse Code Modulation)
  - Linear quantization step
  - Encoded value correspond to the quantized value
- DPCM
  - Encoded value is the difference between the current sample and the previous sample
  - May improve accuracy and resolution (e.g. having a 16-bit dynamic range without having to encode 16-bit samples)
- ADPCM
  - DPCM with a non-linear quantization step
  - May achieve better SNR (Signal/Noise Ratio)

Analog / Digital Conversion Trade-offs

- Low sampling rates and small precision mean conversion errors
  - Lower cost
  - Enough for some applications



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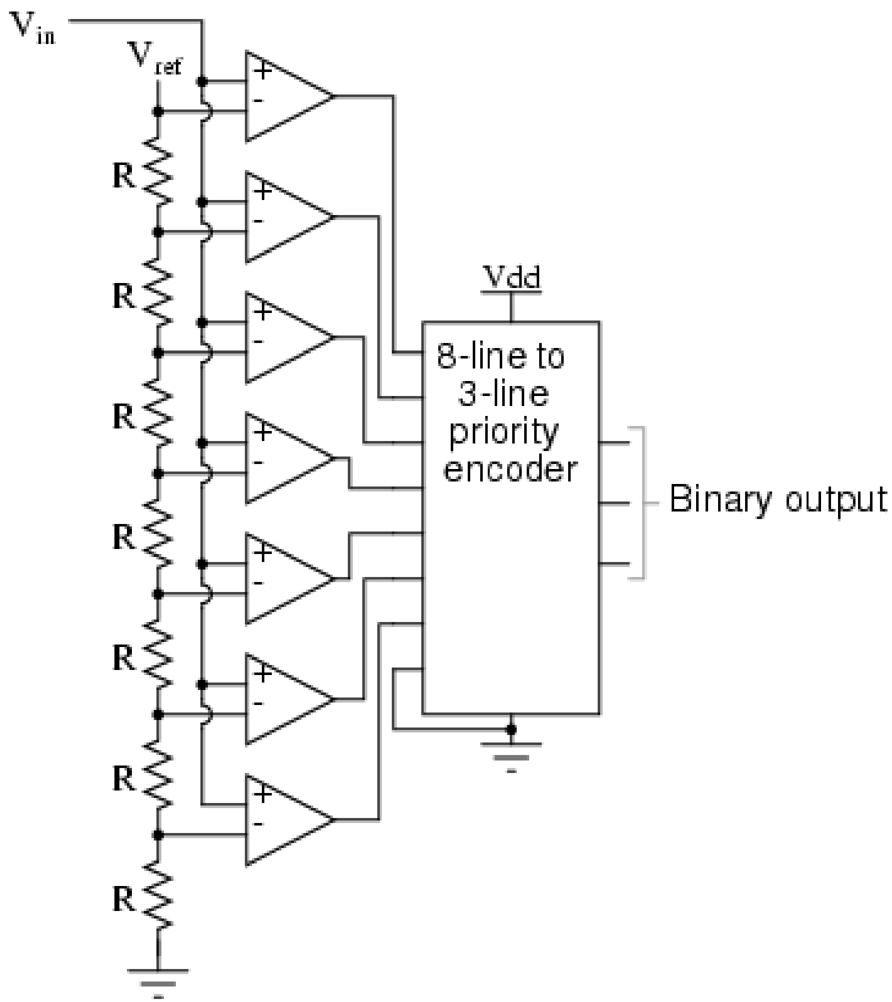
Analog / Digital Conversion Tradeoffs

- High sampling rates and resolution mean better conversion
  - High cost
  - Higher bandwidth
  - Bandwidth example (in bytes/sec):
    - Remember: resolution = amplitude / size
    - Nyquist: sampling rate > 2 x f

		Sampling Rate (Hz)			
		1000	10000	20000	44100
Size (Bytes)	4	500	5000	10000	22050
	6	750	7500	15000	33075
	8	1000	10000	20000	44100
	10	1250	12500	25000	55125
	16	2000	20000	40000	88200

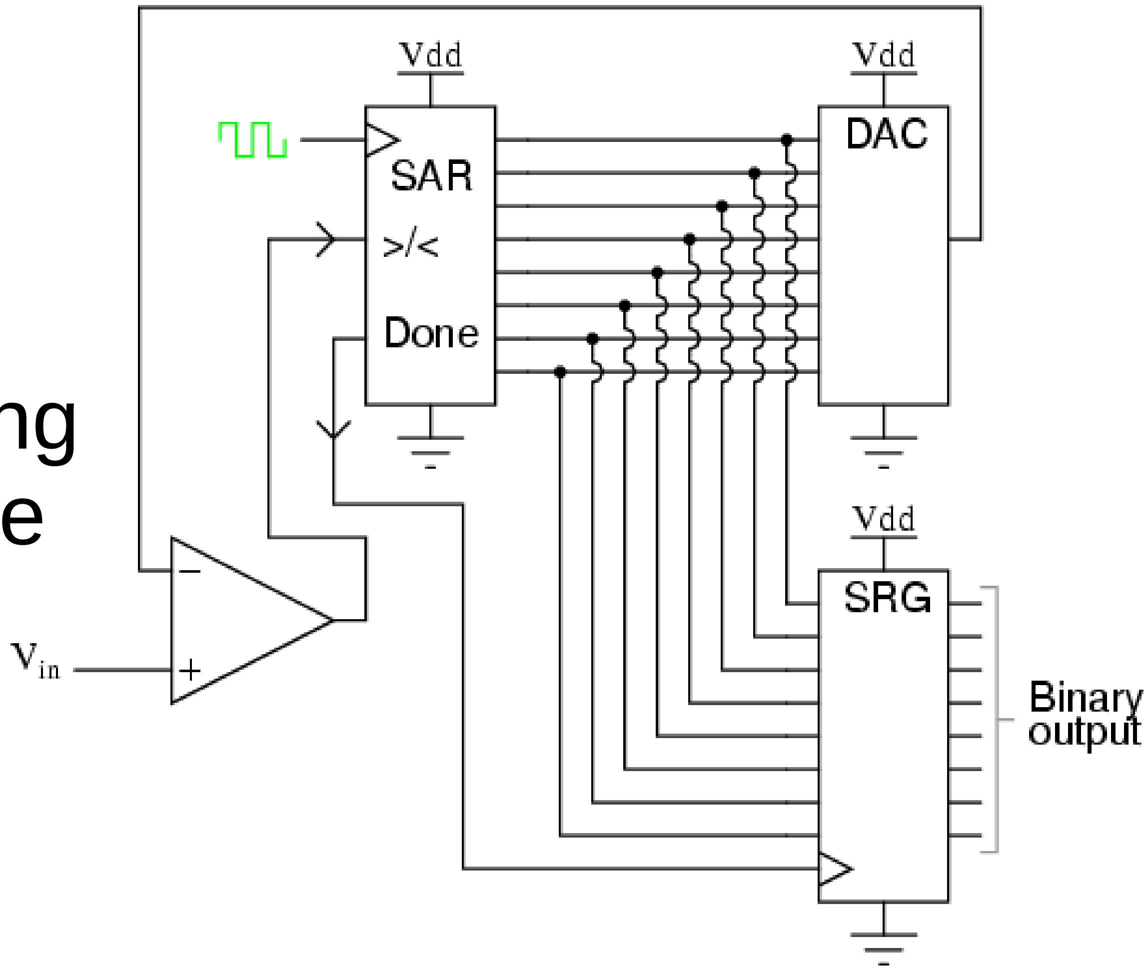
Flash ADC

- One comparator associating each tension level with an output digital word
- A 2-bit Flash ADC needs 4 comparators, a 4-bit, 16, and so forth
- Very fast, but limited precision



Successive-approximation ADC

- Uses a comparator to reject ranges of voltages, eventually settling on a final voltage range



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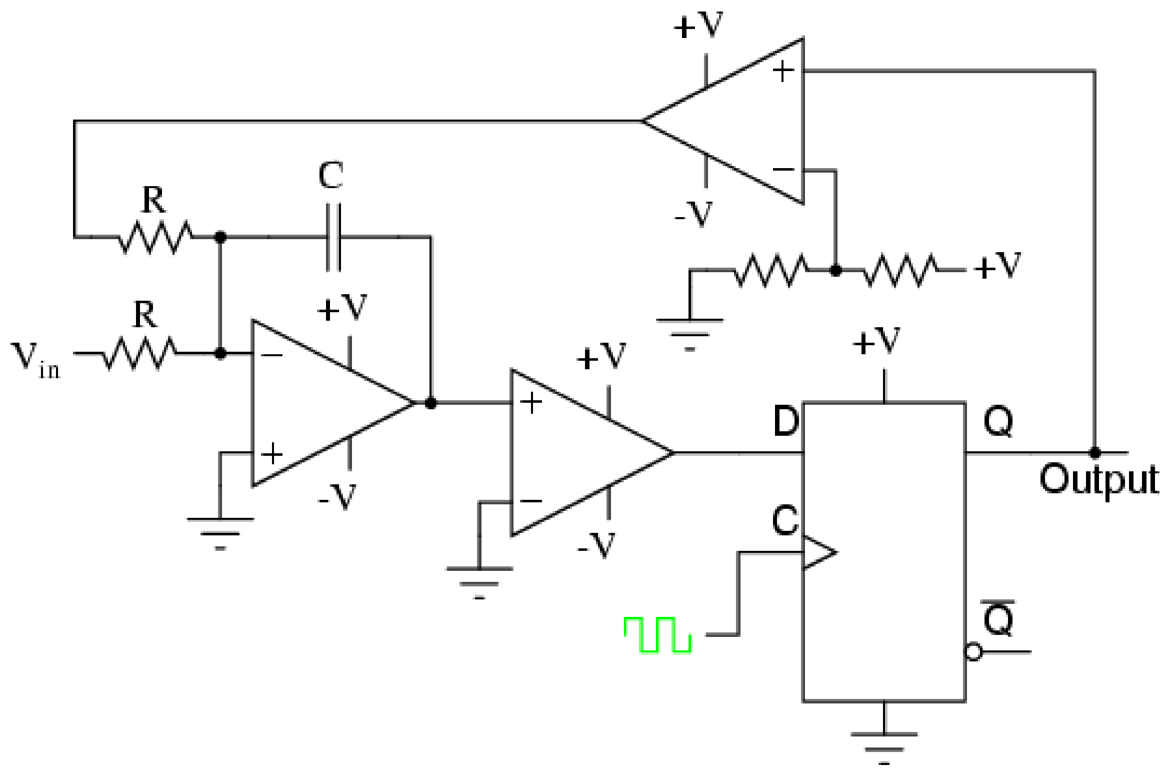
Delta-Sigma ADC

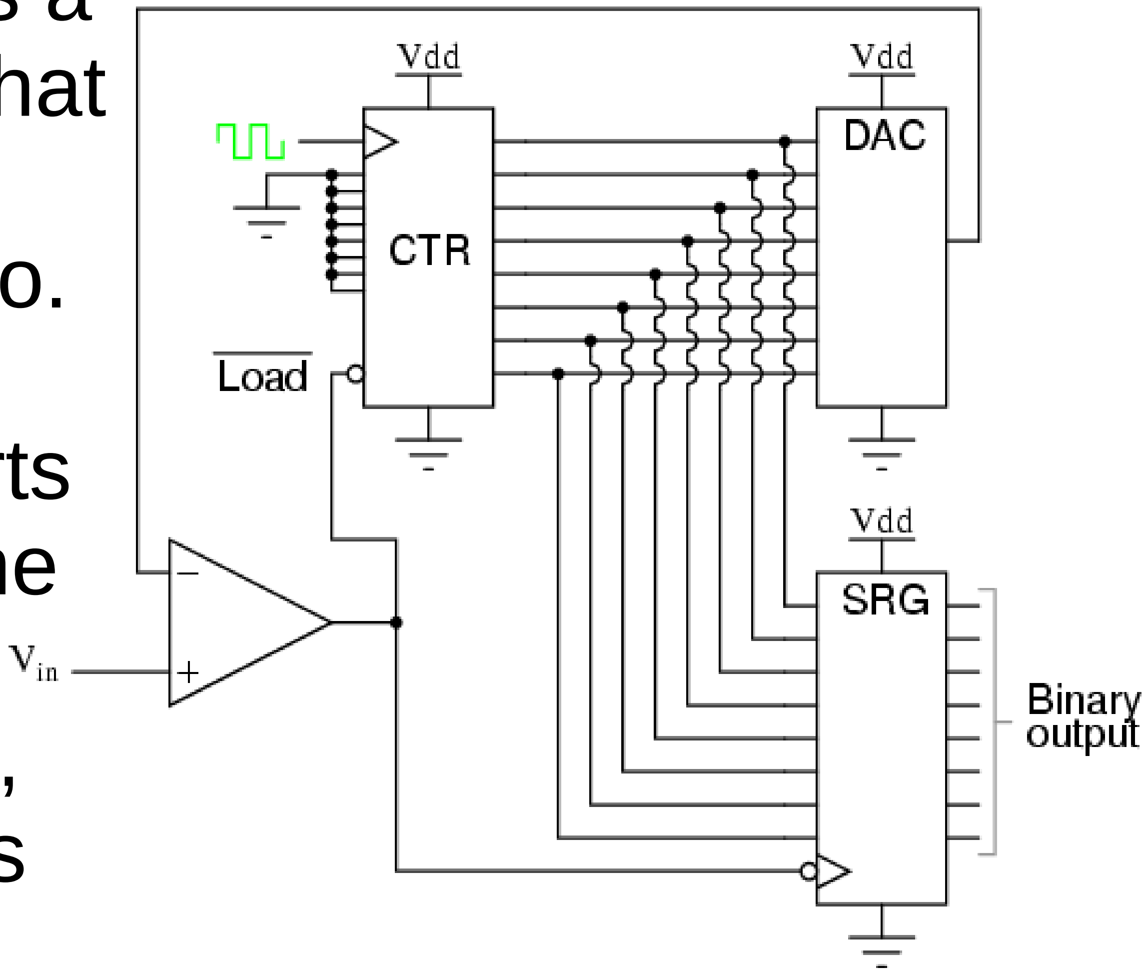
- Analog input signal connected to integrator
- Ramping voltage compared to ground
  - 1-bit ADC



- Comparator output latched through a D-type flip-flop clocked at a high frequency
- Fed back to integrator

Ramp-Compate ADC

- For each sample, the ADC produces a saw-tooth signal that ramps up, then quickly falls to zero. When the ramp starts, a timer starts counting. When the ramp voltage matches the input, the timer's value is recorded



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Analog / Digital Converters

Conversion Type	Typical Sampling Rate	Typical Precision
Flash	5Mhz – 500Mhz	4-8 bits
Successive Approx.	50Khz – 5Mhz	8-10 bits
Sigma-Delta	10Khz – 10Mhz	10-16 bits
Ramp-Compare	1Hz – 1 Khz	10-20 bits

ADC: Operational Parameters

- Conversion range
  - Determines the amplitude of the analog signal
  - May be fixed or selectable
  - Usually determined by a GND and a Vref voltage
  - An analog value that is equal to GND will determine a 0 output in the ADC
  - A Vref analog value will determine a MAX output in the ADC
  - The larger the analog signal amplitude, the bigger the quantization step
- Differential and Single-ended conversion
  - The first measures the difference between signals
  - The second measures a single analog signal

ADC: Operational Parameters

- Operation Frequency
  - Maximum is determined by the manufacturer
  - Internal or external clocks
  - Determines sampling rate
  - High frequencies imply on higher temperatures
- Bandwidth
  - Output speed
  - Sampling Rate = Frequency / Conversion Cycles
  - BW = Sampling rate / 2   (Nyquist)

ADC: Errors

- Absolute error
  - Maximum deviation between the actual ant the ideal ADC transfer functions. Composed by:
    - quantization error (+/- ½ LSB)
    - offset error
    - gain error
    - non-linearity
- Offset error
  - When a transition from 0 to 1 does not occur at an input value of ½ LSB
  - Offset error = Input voltage at the first 0 to 1 transition - Ideal transfer function value at first 0 to 1

ADC: Errors

- Gain error
  - Transfer function slope deviates from the ideal slope
- Non-linearity
  - Variation in the width of quantization steps
  - Maximum difference between the ideal width and each step width
- Calibration and compensation
  - Offset, gain and non-linearity errors may be measured and compensated
  - Important for high-precision devices

Digital / Analog Conversion

- Translates a binary input code to an analog output voltage
- Similar principle to ADCs
- Different conversion speeds and input rates
  - Expensive devices x glitches
- Examples
  - Pulse Width Modulator (PWM)
  - Delta-Sigma
  - R-2R Ladder

ADCs and DACs in Embedded Systems

- Devices
  - External
    - Parallel (GPIO)
    - Serial (SPI, I2C)
    - Myriad of choices, Requires additional circuitry
  - Internal (MCU-embedded)
    - Register-controlled
    - Limited choices, Easy to interface
  - Software ADCs
    - Built with an internal analog comparator and some additional circuitry
    - Limited precision/sampling rate, cheap

ADC Case Study: Analog Devices AD9260

- 16-bit, Single-channel, up to 2.5 Mhz ADC
- General Purpose, medium/high precision device
- Parallel output
- Additional pins for signals
  - Data available, Overflow
- Configuration
  - Sampling rate (via Input Clock)
  - Conversion range (via Analog Reference Inputs)

ADC Case Study: AVR ATMega ADC

- 10-bit, 8-channel, up to 1 Mhz ADC
  - Conversion
    - 0.5 LSB integral non-linearity, ±2 LSB absolute accuracy
    - 13 - 260 µs conversion time
  - 2 differential input channels
    - Optional gain of 10x and 200x
  - 0 - VCC ADC input voltage range
    - Selectable 2.56V ADC reference voltage
- Operation
  - Analog inputs shared with GPIO ports
  - Clock prescaling (sampling rate)
  - Optional left adjustment for ADC result readout
  - Free running or single conversion modes
    - Interrupt on completion