Intel Quark SoC

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Intel Quark SoC: embedding x86

- The heart of Galileo

- and Edisson
Intel Quark SoC Architecture
Main Features

- x86 core
  - Pentium class CPU @ 400 MHz (deterministic?)
  - 32-bit, little-endian data, 32-bit addresses
  - 16 Kbyte MESI cache
  - 387-like FPU (no SIMD such as MMX)

- Memory controller
  - DRAM
    - single-channel DDR3 with ECC
    - from 128 MByte to 2 Gbyte
  - SRAM
    - on-die 512 Kbyte with ECC
    - can be mapped entirely or per-page as an overlay

- Security
  - On-die boot ROM with Hardware Root of Trust (RoT)
Main Features

- **Power management**
  - ACPI 3.0 (with S0, S3, and S4/S5)

- **I/O**
  - AMBA
    - Ethernet, USB, SD, I2C master, SPI master, UART
    - 16 GPIO pins (6 powered in S3 for wake up)
  - Legacy
    - SPI for firmware flash
    - Power management controller
    - IC, RTC, HPET, APIC, SPI

- **PCle**

- **Boot up**
  - Legacy PC from the hardware perspective
  - ROT/UEFI from the firmware perspective
Bus Hierarchy
Memory Management

Effective Address Calculation

Index

Base

Displacement

Scale 1, 2, 3, 4

+ Effective Address

Segmentation Unit

Logical or Virtual Address

Descriptor Index

15 3 2 0

Selector RPL

Segement Register

Linear Address

Paging Unit (optional use)

32

32

Physical Address

BE3#–BE0# A31–A2

Physical Memory
Cache
Co-processor Support

- System Management Mode
  - 16-bit (like real mode)
  - SMI