Software/Hardware Integration

Intel IA32 Architecture Overview

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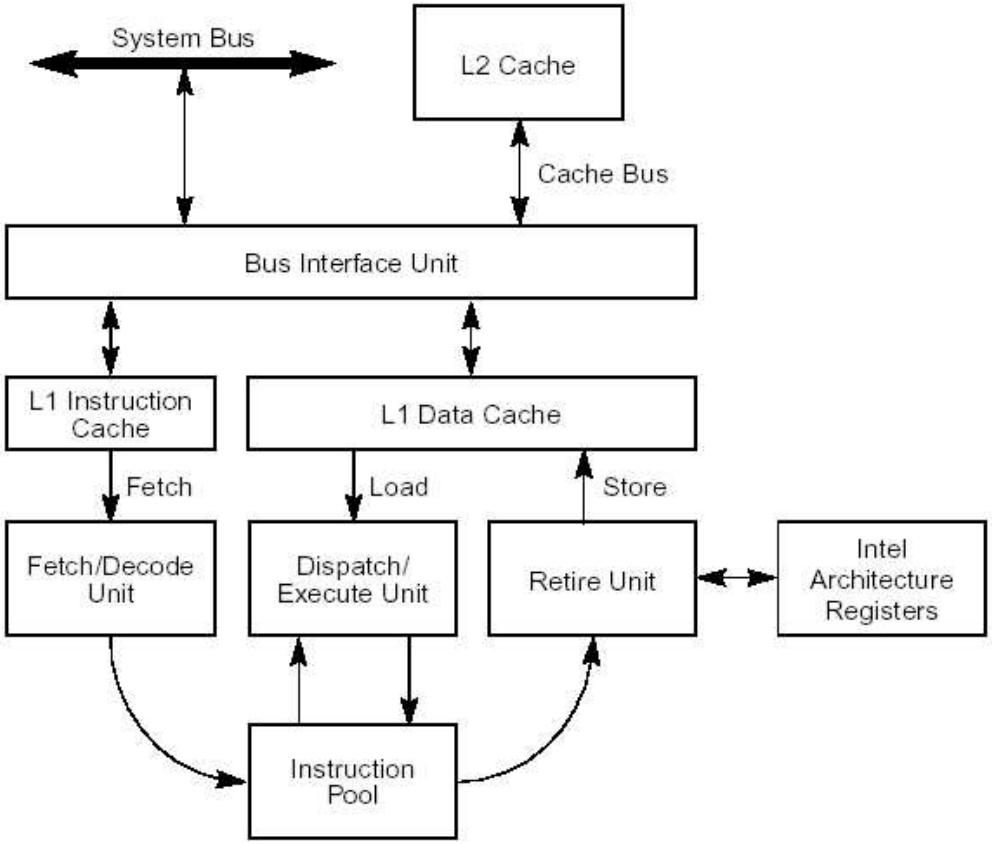
History

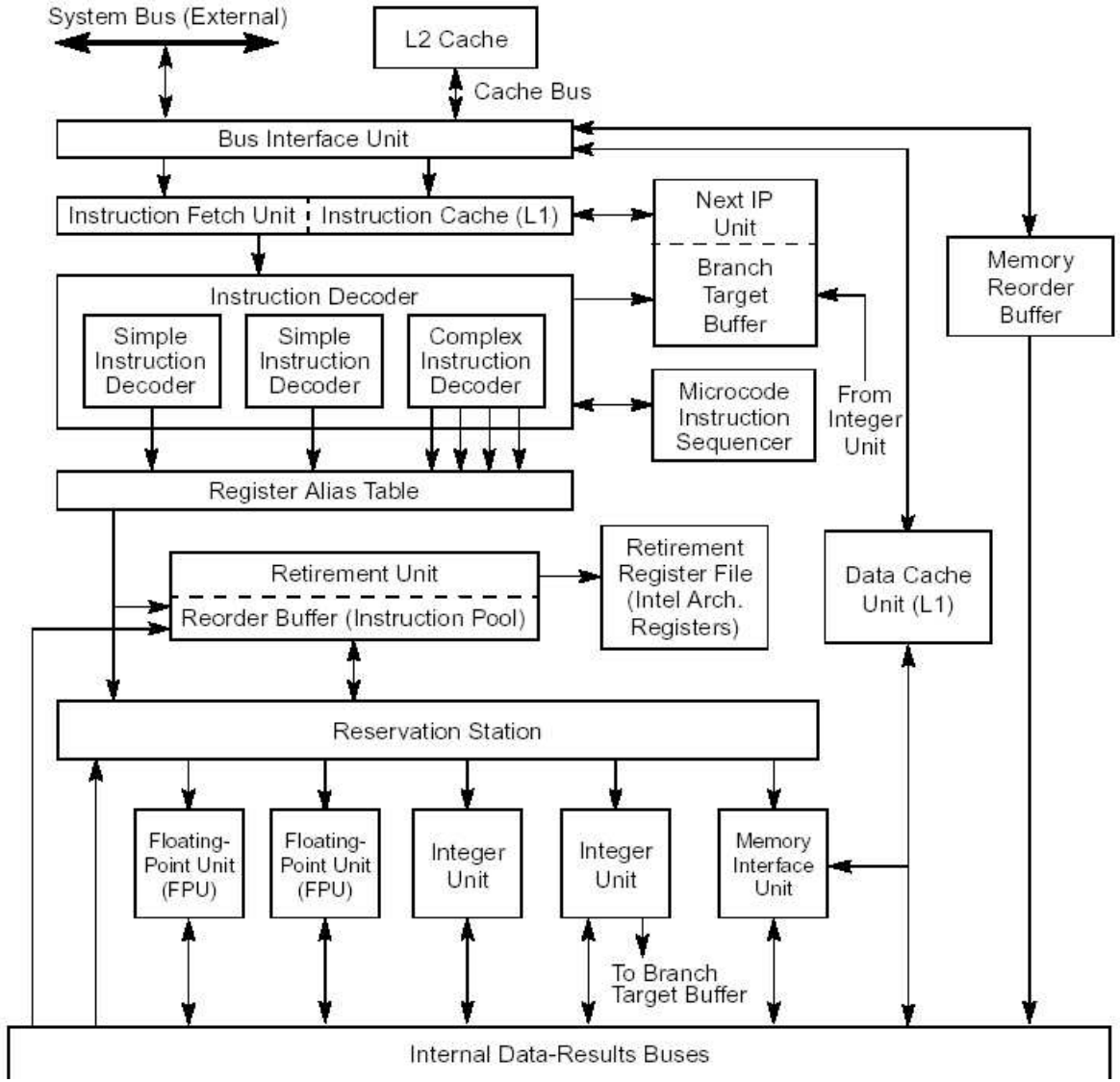
- Successor to the 4004 (8008, 8080, 8085)
- Closely connect to the history of IBM PC and MS DOS

Intel Processor	Date of Product Intro-duction	Perfor-mance in MIPs[1]	Max. CPU Frequency at Intro-duction	No. of Transis-tors on the Die	Main CPU Register Size[2]	Extern. Data Bus Size[2]	Max. Extern. Addr. Space	Caches in CPU Pack-age[3]
8086	1978	0.8	8 MHz	29 K	16	16	1 MB	None
Intel 286	1982	2.7	12.5 MHz	134 K	16	16	16 MB	Note 3
Intel386™ DX	1985	6.0	20 MHz	275 K	32	32	4 GB	Note 3
Intel486™ DX	1989	20	25 MHz	1.2 M	32	32	4 GB	8KB L1
Pentium®	1993	100	60 MHz	3.1 M	32	64	4 GB	16KB L1
Pentium Pro	1995	440	200 MHz	5.5 M	32	64	64 GB	16KB L1; 256KB or 512KB L2

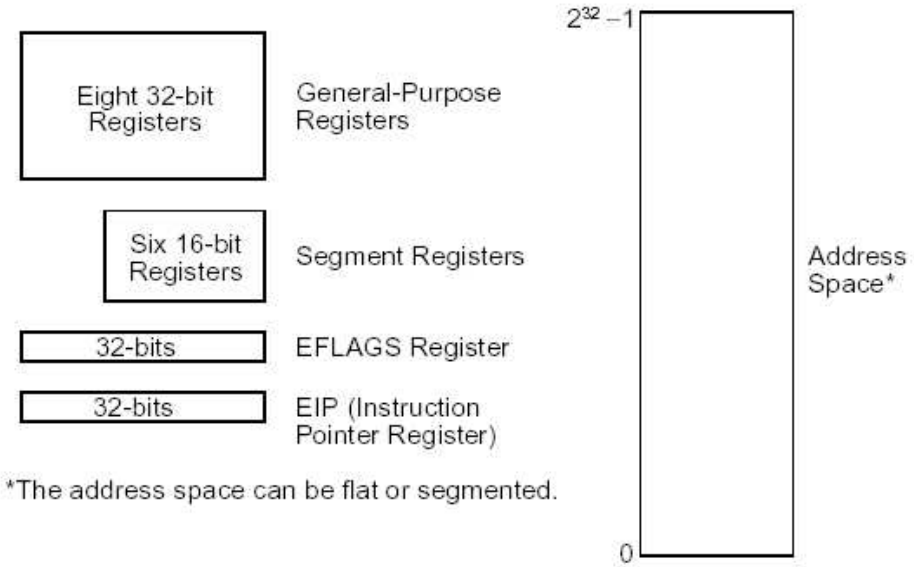
Pipeline Overview

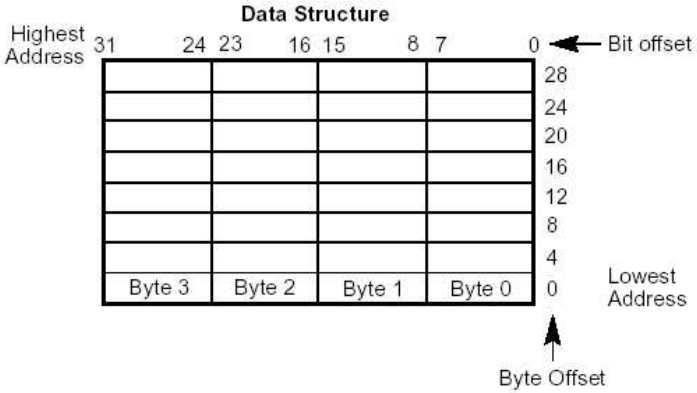


12-Stage Pipeline

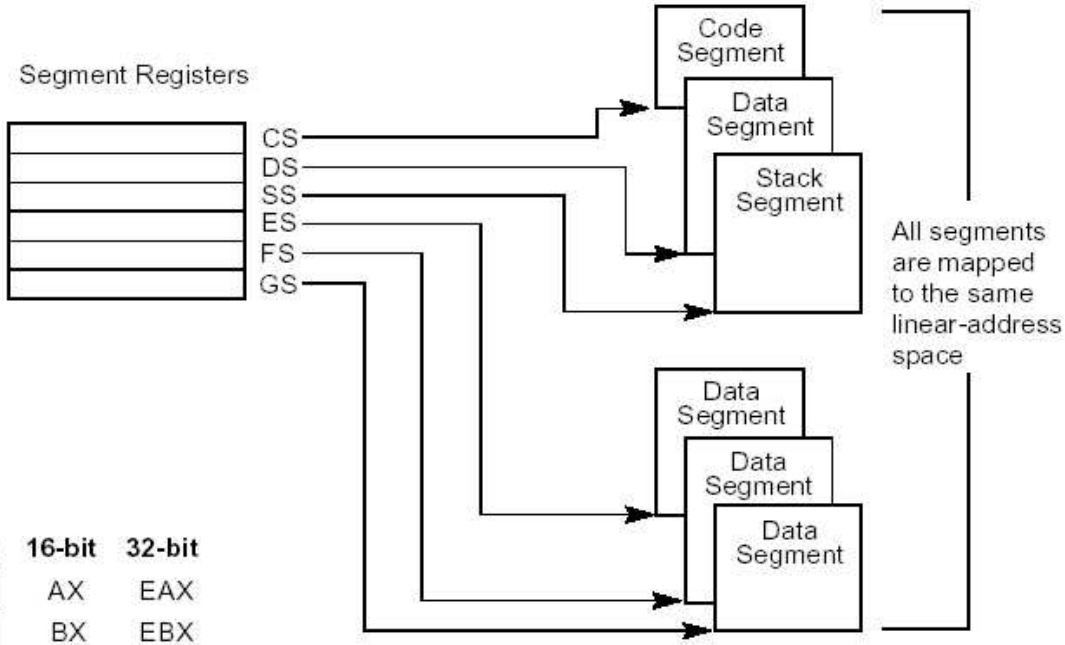


Registers and Memory





Registers



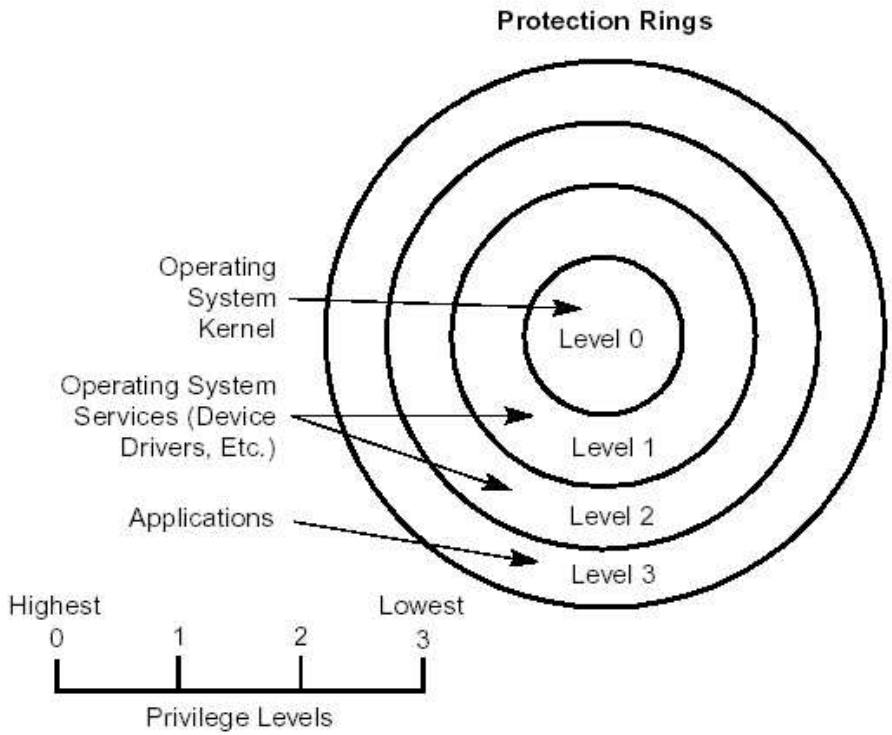
General-Purpose Registers

31 16	15 8	7 0	16-bit	32-bit
	AH	AL	AX	EAX
	BH	BL	BX	EBX
	CH	CL	CX	ECX
	DH	DL	DX	EDX
	BP			EBP
	SI			ESI
	DI			EDI
	SP			ESP

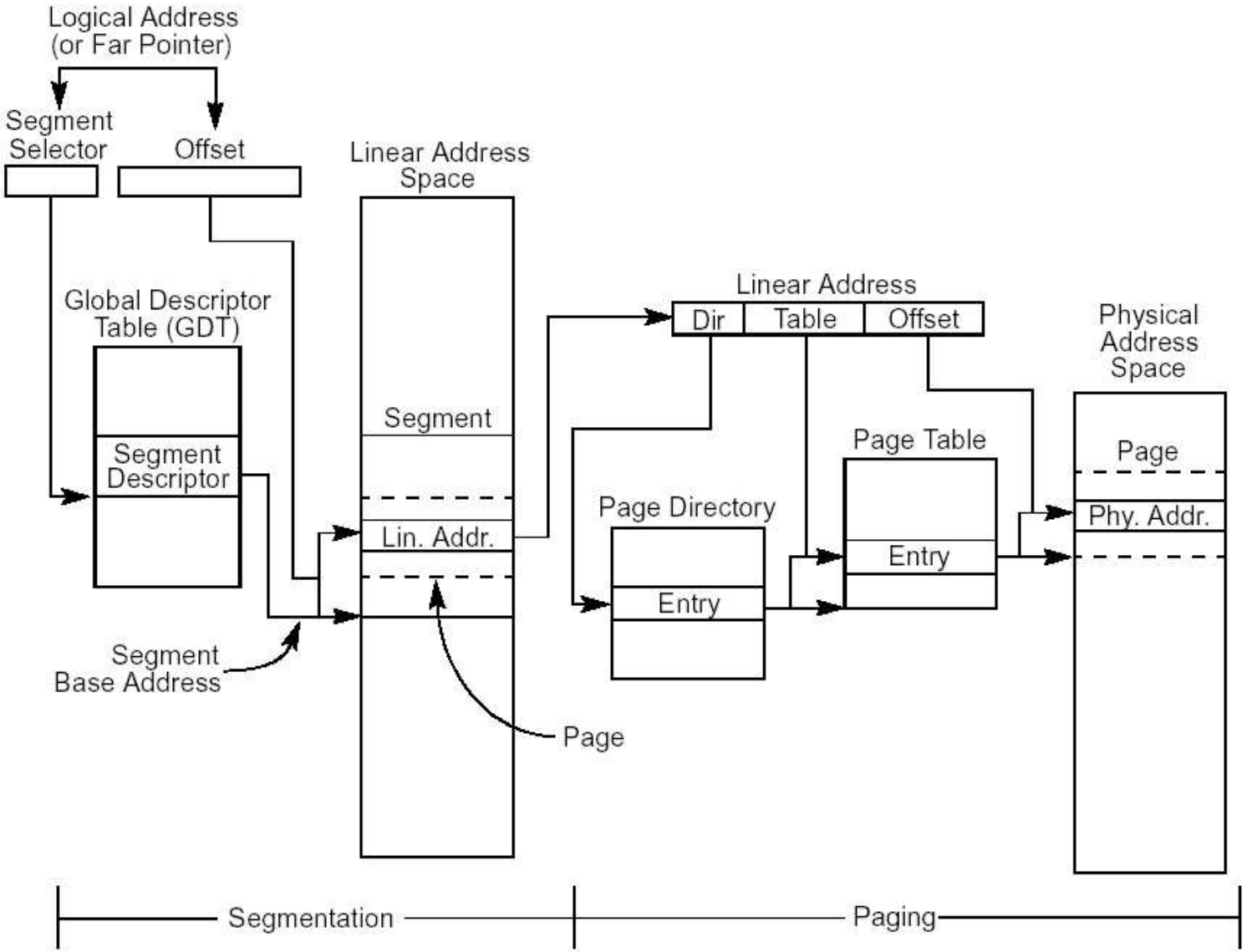
Instruction Set

- Many, many instructions
- Plus
  - String operations (MOVS, CMPS, SCANS)
  - Stack frame mounting (ENTER/LEAVE)
  - Table look up (XLAT)
  - I/O operations (16 bits addresses x 8 bits data)
  - Processor identification (CPUID)
  - Test-and-set lock (XCHG, XADD, CMPXCHG)
  - Context switch (TSS)
  - Floating point (IEEE 754)
  - SIMD Integer Unit (MMX)

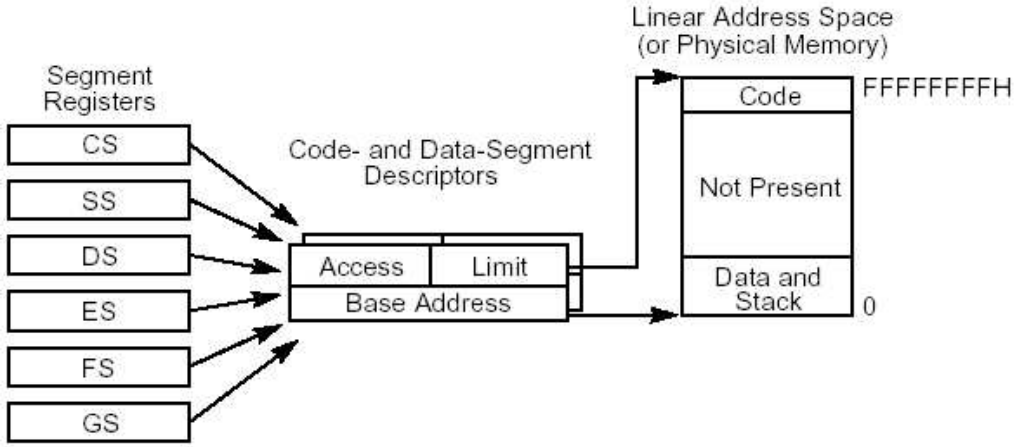
Protection


Protection Rings
Operating System Kernel
Operating System Services (Device Drivers, Etc.)
Applications
Level 0
Level 1
Level 2
Level 3
Highest
Lowest
0
1
2
3
Privilege Levels

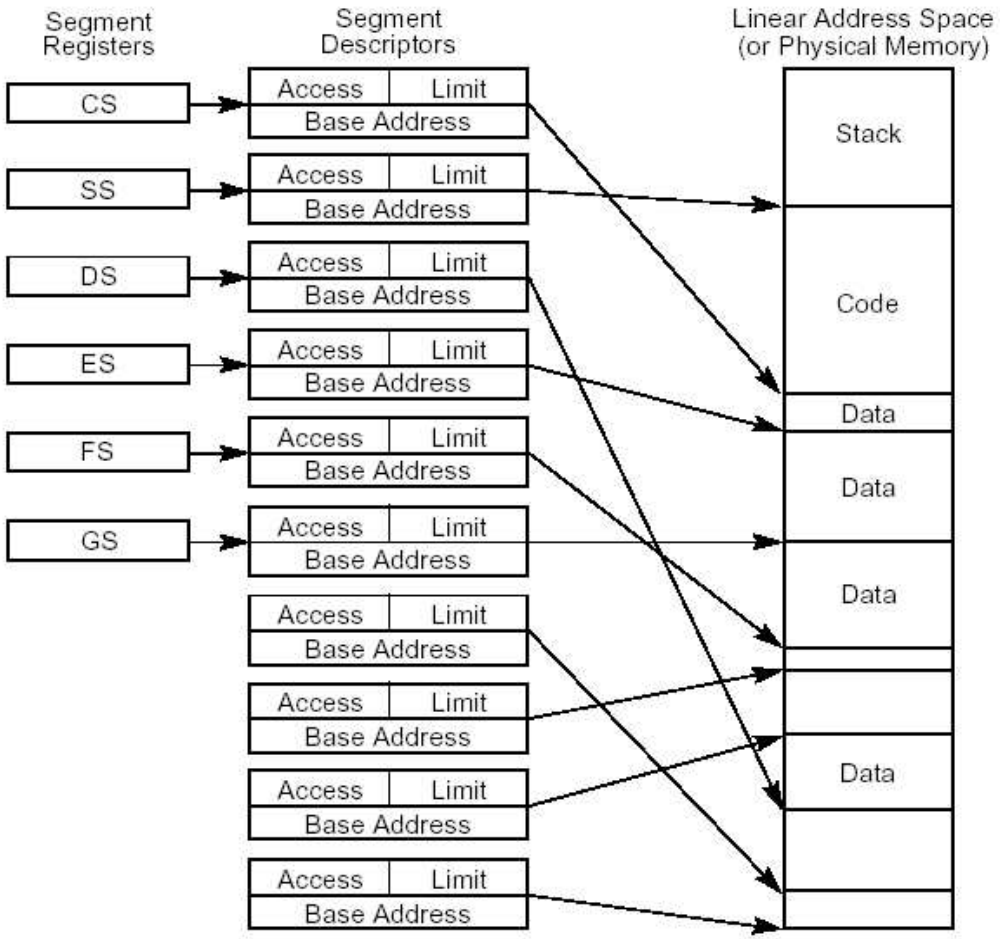
Memory Management



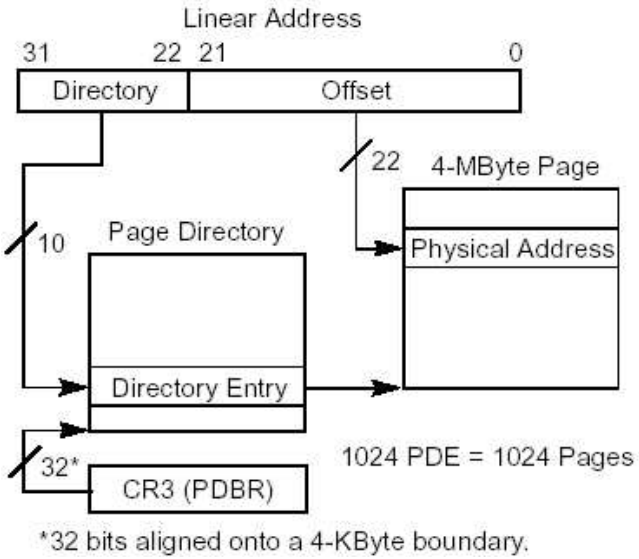
Flat Segmentation

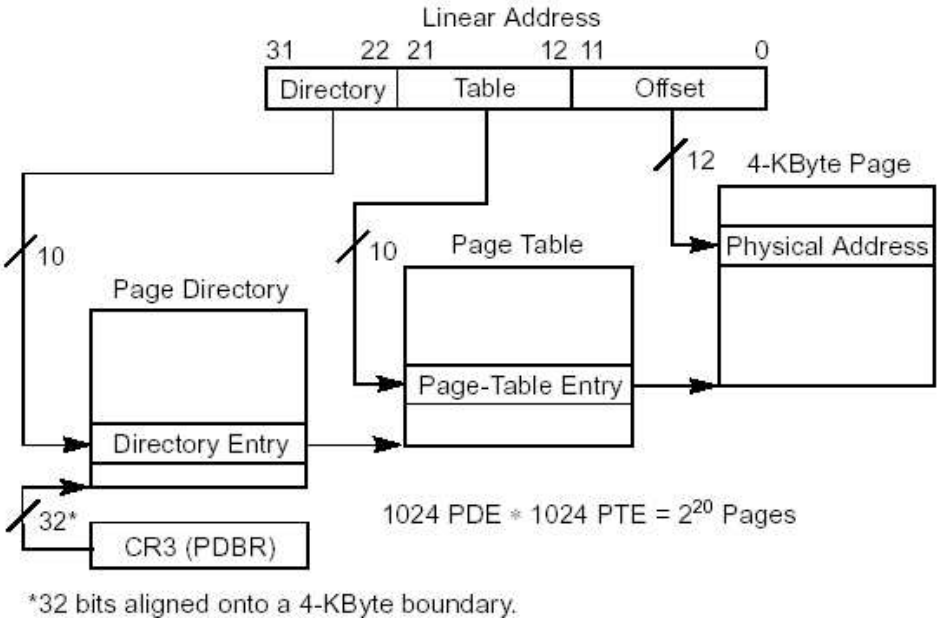


Segmentation



Paging


Linear Address
31
22
21
0
Directory
Offset
22
4-MByte Page
Physical Address
10
Page Directory
Directory Entry
32*
CR3 (PDBR)
1024 PDE = 1024 Pages
*32 bits aligned onto a 4-KByte boundary.


Linear Address
31
22
21
12
11
0
Directory
Table
Offset
12
4-KByte Page
Physical Address
10
Page Table
Page-Table Entry
10
Page Directory
Directory Entry
32*
CR3 (PDBR)
1024 PDE * 1024 PTE = 2^20 Pages
*32 bits aligned onto a 4-KByte boundary.

Interrupt Handling