

System Programming

The SPIM S20 MIPS Simulator

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SPIM S20

- MIPS R2000/R3000 simulator
 - Ignores cache and memory latency
 - Ignores delay of operations (multiplies/divides)
 - Expands pseudo instructions to real machine instructions
 - Self contained system
 - Support of few Operating System services
 - Basic I/O (console)
 - Compilation not necessary
 - Directly interprets assembly

Installing SPIM S20

- The source code is available on the class homepage
- Already installed on Lab computers
- Dependencies
 - Bison: parser generator
 - Flex: lexical analyzer generator
 - Xaw3d: graphical library (X Window version)

Running the Simulator

- Just run command `spim`
- Some useful flags
 - bare: simulate without pseudo-instructions and additional addressing modes
 - asm: simulate the virtual MIPS machine (default)
 - file: Load and execute the assembly code in file
 - ef: Specify the exception handler assembler file

Running an Application

- Application

- Calculates the mean value of an integer array in memory

- Simulation

```
spim -file lab01.asm
```

- Or

- 1) Run Spim: `spim`

- 2) Load application: `(spim) read "lab01.asm"`

- 3) Start the execution of application: `run`

Inspecting Programs Data

■ Registers

- All: `(spim) print_all_regs [hex]`
- Integer register N: `(spim) print $N`
- Floating point register N: `(spim) print $fN`

■ Application Symbols

`(spim) print_symbols`

■ Memory

`(spim) print <ADDR>`

Step by Step and Breakpoints

■ Executing a program step by step

`(spim) step [N]` (**N** is the number of instructions to run)

● Leaving step-by-step mode

`(spim) continue`

■ Breakpoints

● Define points on execution flow that stops the simulation and enter in “step” mode

● Set breakpoint: `(spim) breakpoint <addr>`

● Delete breakpoint: `(spim) delete <addr>`

● List Breakpoints: `(spim) list`

User Interfaces

- Xspim
 - X Window Graphical Interface
 - Provides a operation to change the values of registers/memory locations

- PCSpim
 - Windows version of SPIM
 - Tutorial available at <http://www.inf.ufsc.br/~cancian/personal/arquitetura.html>

System Programming

The SPIM Assembler

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MIPS Register Usage

- Defined in Application Binary Interface (**ABI**)
 - **Low-level interface** between Application and Operating System

Register Name	Number	Usage
\$zero	0	Constant ZERO
\$at	1	Assembly reserved
\$v0-1	2-3	Expression Evaluation and result of function
\$a0-3	4-7	Arguments
\$t0-7	8-15	Temporary (not preserved across call)
\$s0-7	16-23	Saved temporary (preserved across call)
\$t8-9	24-25	Temporary (not preserved across call)
\$k0-1	26-27	Reserved for OS kernel
\$gp	28	Pointer to global area
\$sp	29	Stack Pointer
\$fp	30	Frame Pointer
\$ra	31	Return Address

SPIM Assembler Directives

Directive	Function
<code>.data <addr></code>	Start a data segment, optionally specify an <code><addr></code>
<code>.text <addr></code>	Start a text segment, optionally specify an <code><addr></code>
<code>.globl sym</code>	Declare global symbol <code>sym</code>
<code>.align n</code>	Align next allocation pointer in 2^n bytes
<code>.space n</code>	Skip the allocation pointer in <code>n</code> bytes
<code>.byte b_1, \dots, b_n</code>	Initialize <code>n</code> byte size data
<code>.half h_1, \dots, h_n</code>	Initialize <code>n</code> half-word size data
<code>.word w_1, \dots, w_n</code>	Initialize <code>n</code> word size data
<code>.float f_1, \dots, f_n</code>	Initialize <code>n</code> single precision floating-point data
<code>.double d_1, \dots, d_n</code>	Initialize <code>n</code> double precision floating-point data
<code>.ascii str</code>	Initialize a ASCII <code>str</code>
<code>.asciiz str</code>	Initialize a ASCII <code>str</code> and null-terminate it

MIPS Architecture

- Load/Store Architecture
- Bare machine provides only `imm(register)` for memory addressing
- Pseudo-instructions supports more 5 memory-addressing mode

<code>(register)</code>	opcode (\$gp)
<code>imm</code>	opcode 100
<code>label</code>	opcode array
<code>label +/- imm</code>	opcode array + 8
<code>label +/- imm(register)</code>	opcode array + 8 (\$gp)

Basic Data Operations

- Move data between registers
- Use
Move temporary register
to a specific purpose
register
Eg. Function arguments

Data Movement
`move rd, rs`
`rd <- rs`

	Memory	Registers
100	10	rd 5
102	20	rs 8
104	30	rt 9
106	40	
108	50	

Basic Data Operations

- Move data between registers
- Use
Move temporary register
to a specific purpose
register
Eg. Function arguments

Data Movement
`move rd, rs`
`rd <- rs`

	Memory	Registers
100	10	rd 8
102	20	rs 8
104	30	rt 9
106	40	
108	50	

Basic Data Operations

- Sum data in registers

Sum Data
`add rd, rs, rt`
 $rd \leftarrow rs + rt$

- Use
 Basic calculations

- Related Opcodes
`addu` – ADD Unsigned
 Do not generate a
 overflow exception

	Memory	Registers
100	10	rd <input type="text" value="5"/>
102	20	rs <input type="text" value="8"/>
104	30	rt <input type="text" value="9"/>
106	40	
108	50	

Basic Data Operations

- Sum data in registers
- Use
Basic calculations
- Related Opcodes
`addu` – ADD Unsigned
Do not generate a
overflow exception

Sum Data
`add rd, rs, rt`
 $rd \leftarrow rs + rt$

	Memory	Registers
100	10	rd 17
102	20	rs 8
104	30	rt 9
106	40	
108	50	

Basic Data Operations

- Sum data in register and a 16 bits value

Sum Data
`addi rt, rs, imm`
 $rt \leftarrow rs + imm$

- Use

Basic calculations
 Initialization of values

- Related Opcodes
`addiu` – ADD Immediate
 Unsigned
 Do not generate a
 overflow exception

	Memory	Registers
100	10	rd <input type="text" value="5"/>
102	20	rs <input type="text" value="8"/>
104	30	rt <input type="text" value="9"/>
106	40	Immediate
108	50	<input type="text" value="-50"/>

Basic Data Operations

- Sum data in register and a 16 bits value

Sum Data
`addi rt, rs, imm`
 $rt \leftarrow rs + imm$

- Use

Basic calculations
 Initialization of values

- Related Opcodes

`addiu` – ADD Immediate

Unsigned

Do not generate a
 overflow exception

	Memory	Registers
100	10	rd 5
102	20	rs 8
104	30	rt -42
106	40	Immediate
108	50	-50

Memory Access Instructions

- Load a 16 bits value in a register

Load Immediate

`li rt, imm`

`rt <- imm`

- Use Initialization of values

- Related Opcodes

`lui` – Load Upper Immediate

`rt <- imm << 16`

	Memory	Registers
100	10	rd <input type="text" value="5"/>
102	20	rs <input type="text" value="8"/>
104	30	rt <input type="text" value="9"/>
106	40	Immediate
108	50	<input type="text" value="-50"/>

Memory Access Instructions

- Load a 16 bits value in a register

- Use Initialization of values

- Related Opcodes

lui – Load Upper Immediate

$rt \leftarrow imm \ll 16$

Load Immediate

li rt, imm

$rt \leftarrow imm$

	Memory	Registers
100	10	rd <input type="text" value="5"/>
102	20	rs <input type="text" value="8"/>
104	30	rt <input type="text" value="-50"/>
106	40	Immediate
108	50	<input type="text" value="-50"/>

Memory Access Instructions

- Load a 16 bits value in a register

- Use Initialization of values

- Related Opcodes

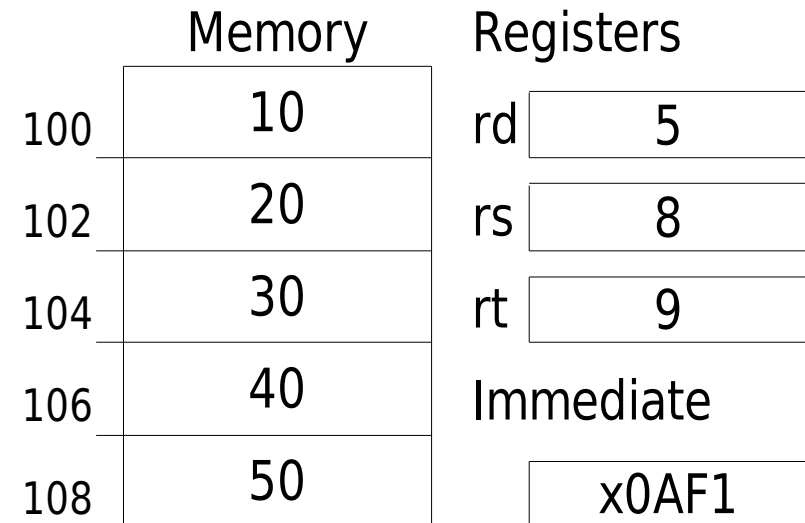
lui – Load Upper Immediate
Immediate

$rt \leftarrow imm \ll 16$

Load Upper Immediate

lui *rt*, *imm*

$rt \leftarrow imm \ll 16$



Memory Access Instructions

- Load a 16 bits value in a register

- Use Initialization of values

- Related Opcodes

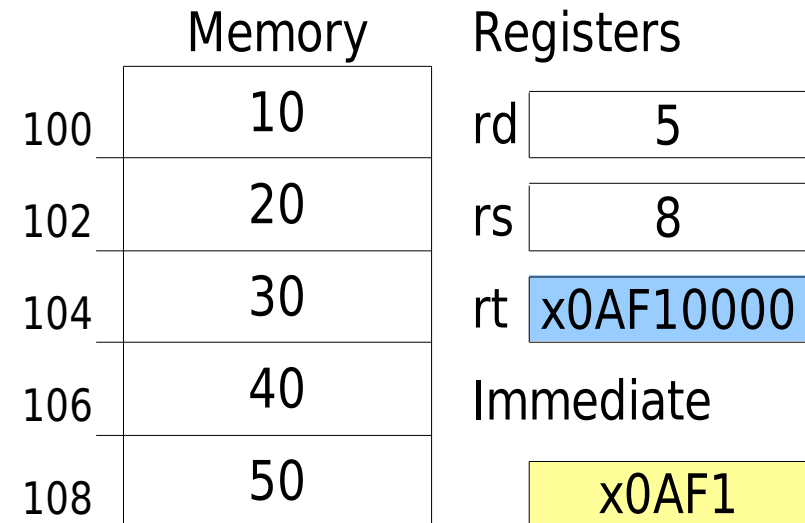
lui – Load Upper Immediate

$rt \leftarrow imm \ll 16$

Load Upper Immediate

lui *rt*, *imm*

$rt \leftarrow imm \ll 16$



Memory Access Instructions

- Load a 32 bits value in a register
- Use Initialization of values

Load Address
`la rt, value`
`rt <- value`

100	10	rd	5
102	20	rs	8
104	30	rt	9
106	40	Value	
108	50		100

Memory Access Instructions

- Load a 32 bits value in a register
- Use Initialization of values

Load Address
`la rt, value`
`rt <- value`

100	10	rd	5
102	20	rs	8
104	30	rt	100
106	40	Value	
108	50		100

Memory Access Instructions

- Load a word on memory to a register

Load Word
`lw rt, address`
 $rt \leftarrow M[\text{address}]$

- Use
Load data from memory

- Related Opcodes

`lb` – Load byte

`lbu` – Load byte unsigned

`lh` – Load Half-Word

`lhu` – Load Half-Word unsigned

`ld` – Load Double-Word

	Memory	Registers
100	10	rd <input type="text" value="5"/>
102	20	rs <input type="text" value="100"/>
104	30	rt <input type="text" value="9"/>
106	40	Value
108	50	<input type="text" value="2"/>

Memory Access Instructions

- Load a word on memory to a register

Load Word
`lw rt, address`
 $rt \leftarrow M[\text{address}]$

- Use
Load data from memory

- Related Opcodes

`lb` – Load byte

`lbu` – Load byte unsigned

`lh` – Load Half-Word

`lhu` – Load Half-Word unsigned

`ld` – Load Double-Word

	Memory	Registers
100	10	rd 5
102	20	rs 100
104	30	rt 20
106	40	Value
108	50	2

Memory Access Instructions

- Store a word in a register in memory

Store Word
`sw rt, address`
 $M[\text{address}] \leftarrow rt$

- Use
 Store data in memory

- Related Opcodes

`sb` – Load byte

`sh` – Load Half-Word

`sd` – Load Double-Word

	Memory	Registers
100	10	rd <input type="text" value="5"/>
102	20	rs <input type="text" value="100"/>
104	30	rt <input type="text" value="9"/>
106	40	Value
108	50	<input type="text" value="2"/>

Memory Access Instructions

- Store a word in a register in memory

- Use
Store data in memory

- Related Opcodes

sb – Load byte

sh – Load Half-Word

sd – Load Double-Word

Store Word
sw *rt*, *address*
 $M[\text{address}] \leftarrow \text{rt}$

	Memory	Registers
100	10	rd <input type="text" value="5"/>
102	9	rs <input type="text" value="100"/>
104	30	rt <input type="text" value="9"/>
106	40	Value
108	50	<input type="text" value="2"/>

SPIM Assembler

Data Addressing Modes



Mode	MIPS Example Instruction	Meaning
Register	move rt, rs	rt <- rs
Immediate	li rt, imm	rt <- imm
Absolute	lw rt, imm	rt <- M[imm]
Reg. Ind.	lw rt, (rs)	rt <- M[rs]
Reg. Ind. Disp.	lw rt, imm(rs)	rt <- M[rs + imm]
Reg. Ind. Ind.	unavailable	-
Reg. Ind. Post-	unavailable	-
Reg. Ind. -Pre	unavailable	-
Reg. Ind. Scal.	unavailable	-
Reg. Ind. Disp. Scal.	unavailable	-
Memory Ind.	unavailable	-