# Computer Architecture Group

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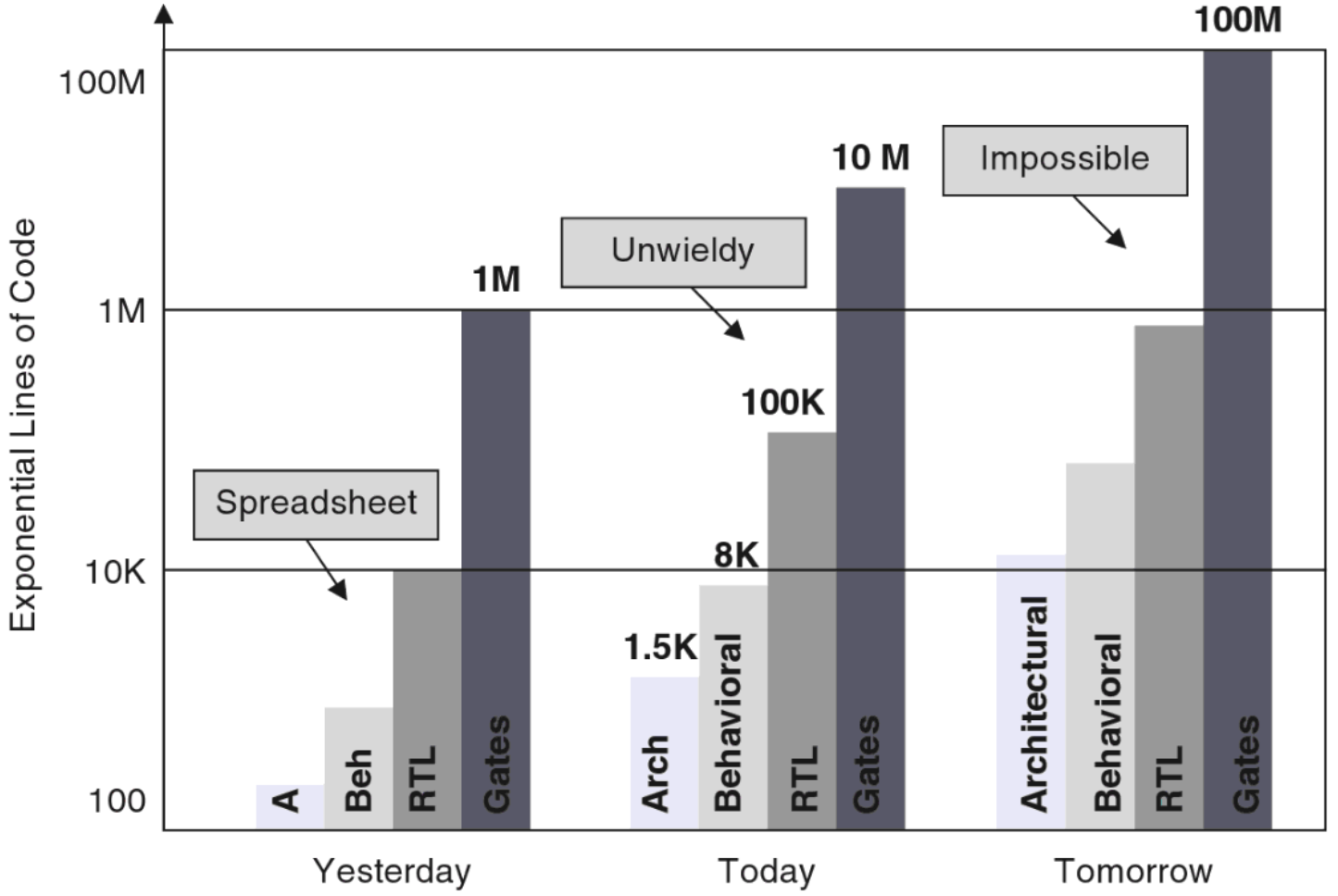
**Msc students:**
- Tiago Rogério Mück
- Wesley Gonçalves

# Introduction

- The complexity systems is always increasing

Code complexity for SoCs designs in various level of abstraction




(Black & Donovan, 2009)

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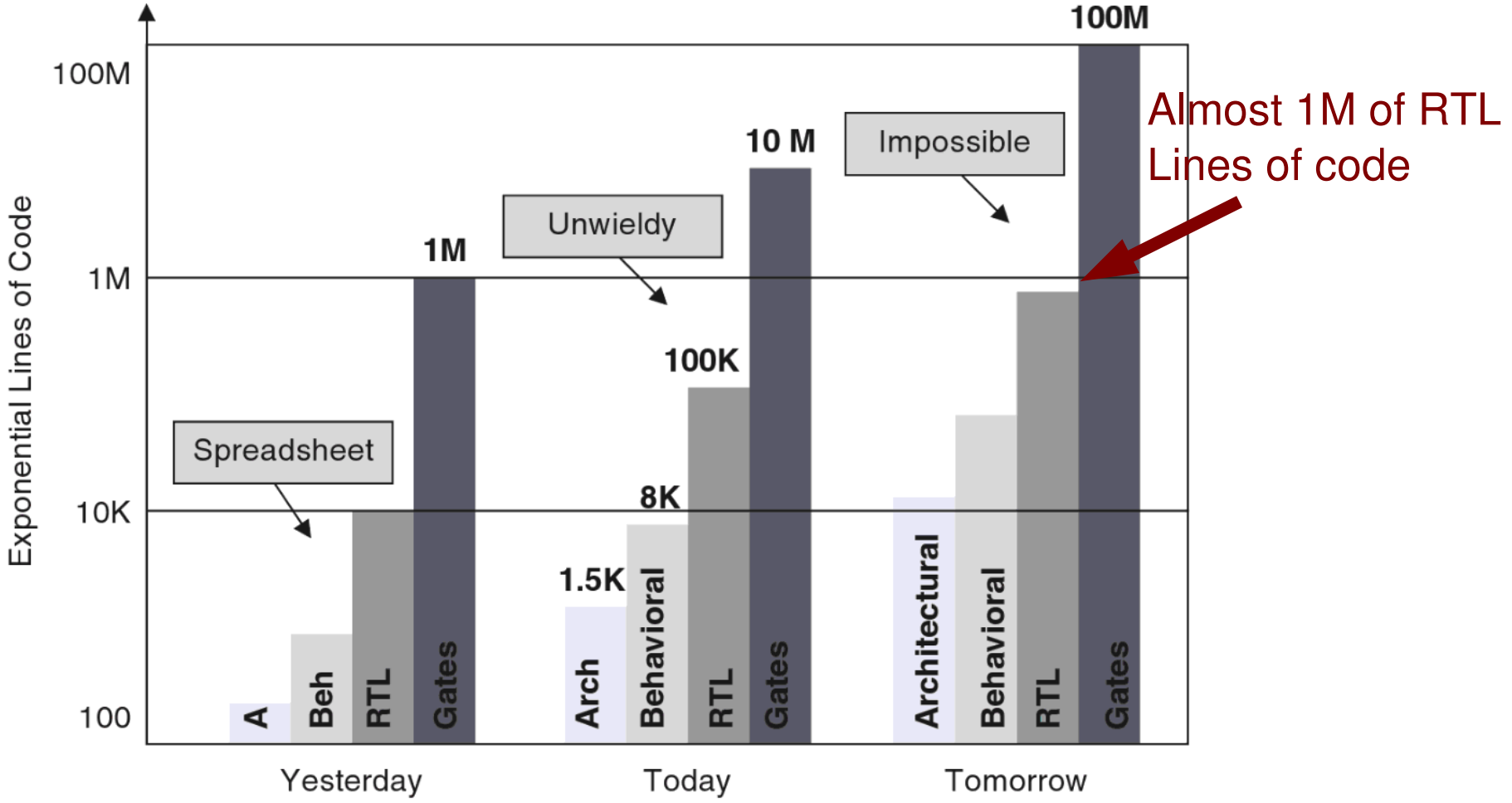


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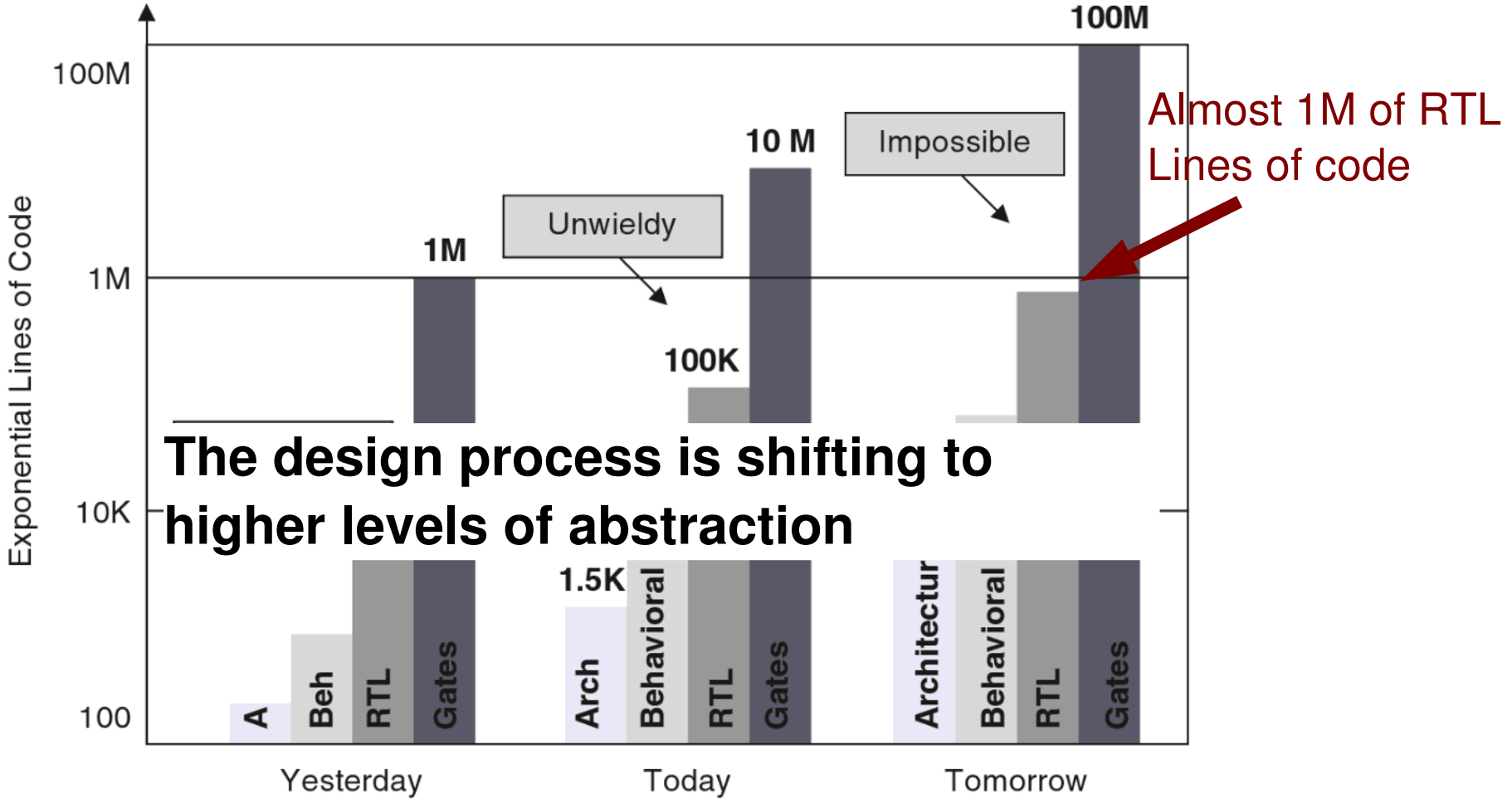


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# Evolution of abstraction levels

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- For software:

```
ADDI $SP, $SP, -8
SW   $A0, 4($SP)
SW   $RA, 0($SP)
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Machine language

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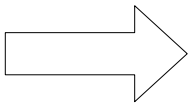

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For (int i = 0; i < 10; ++i)
     do_something(i);
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Procedural language

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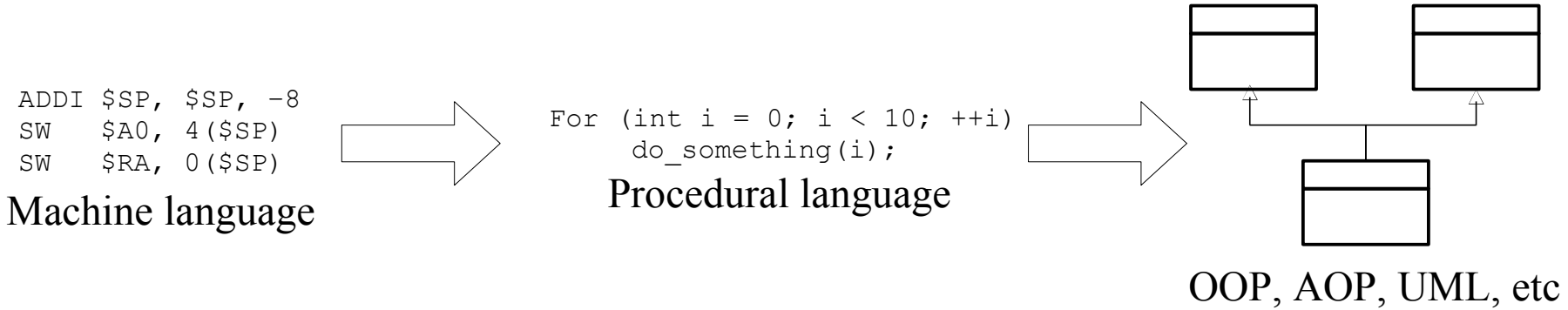

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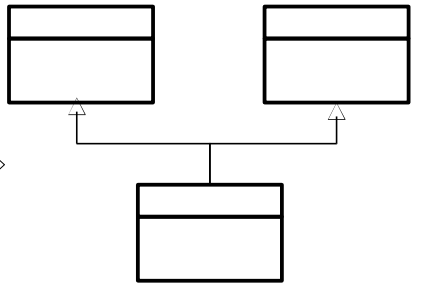
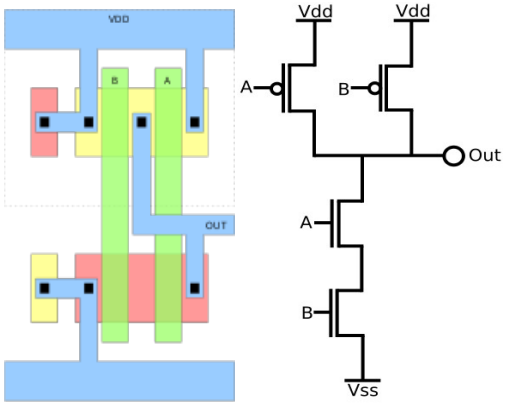


OOP, AOP, UML, etc

- For hardware:




Electric level

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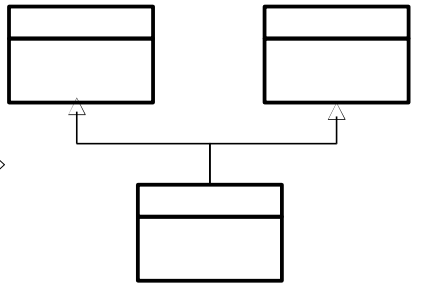

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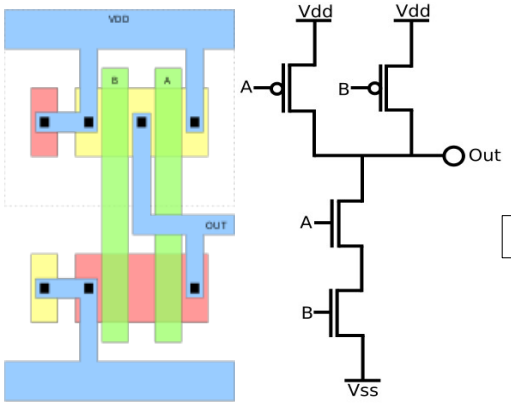





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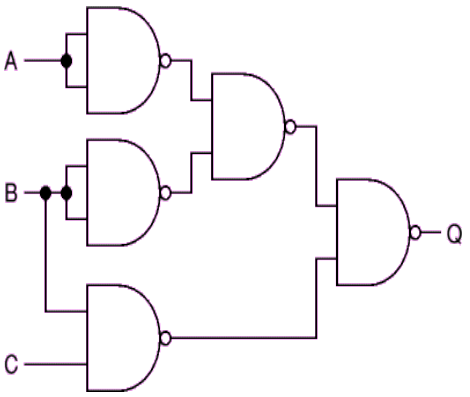


Gate level

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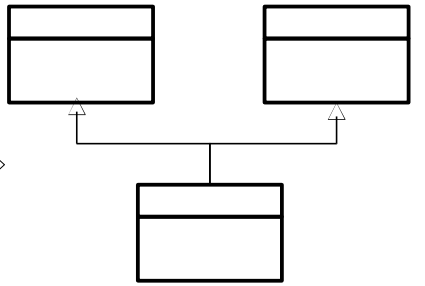

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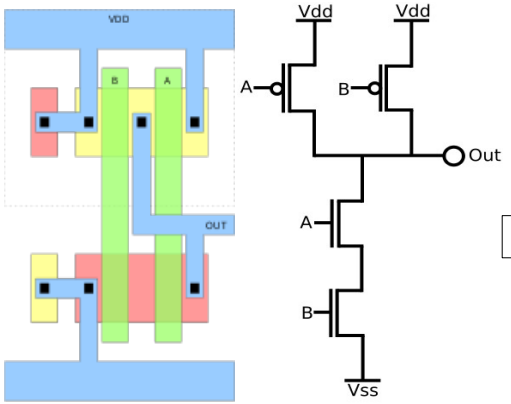





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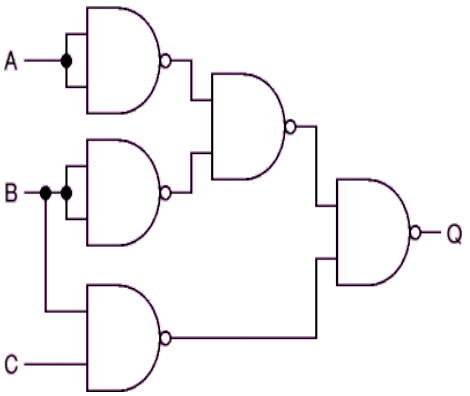


Gate level

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always @(sel or a or b)
begin
  if (sel == 1)
    f = a;
  else
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```

Register transfer level

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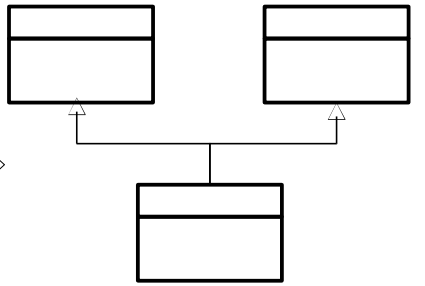
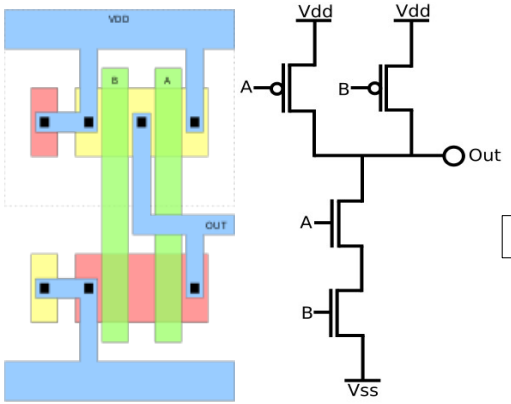


OOP, AOP, UML, etc

- For hardware:

High-level synthesis

High-level modeling

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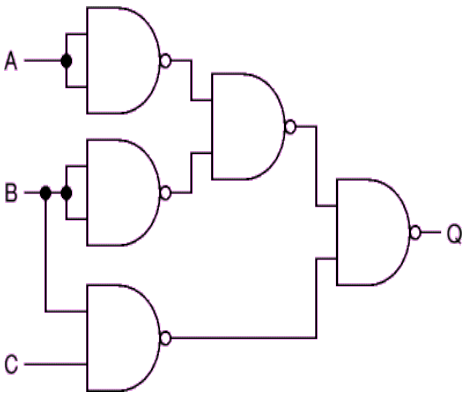


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**Convergence between hardware and software design**

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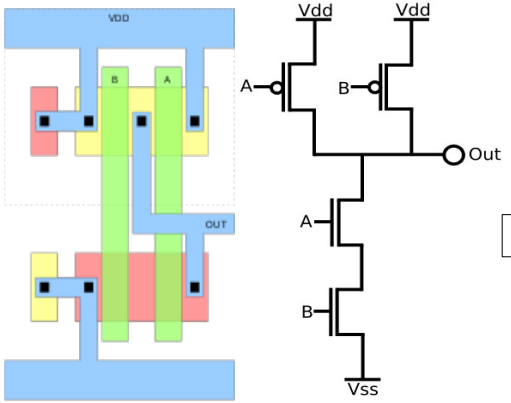


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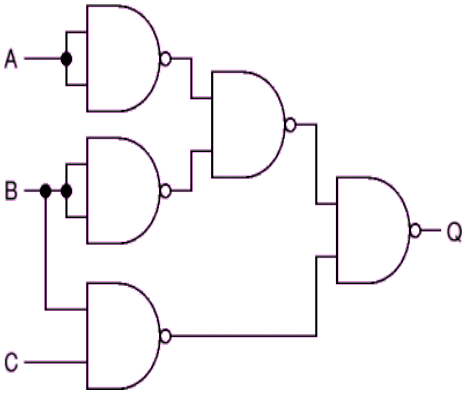


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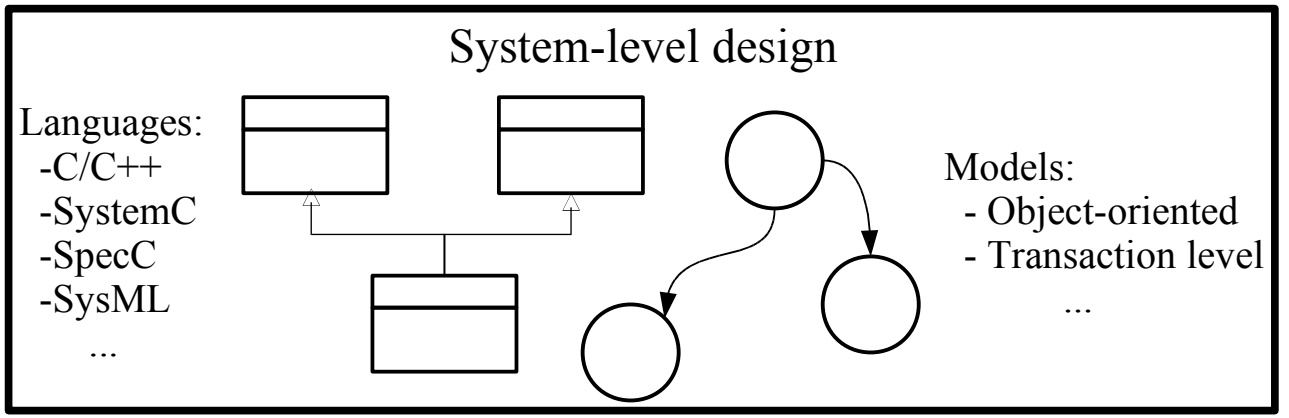
Register transfer level

# System-level design


- Use a single high-level language to provide a model of the whole system which is then refined down to the final implementation

# Today's System-level design flow



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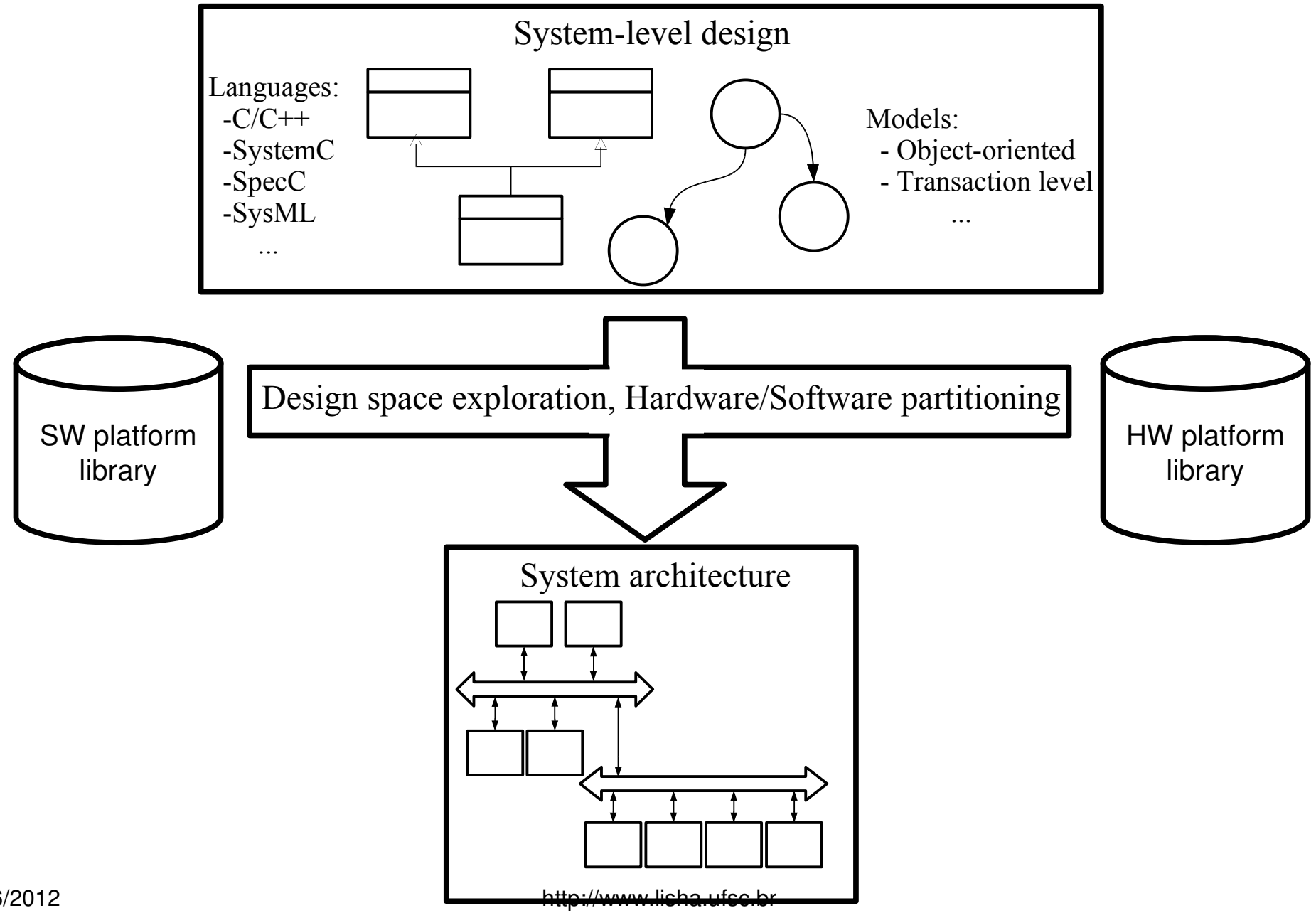

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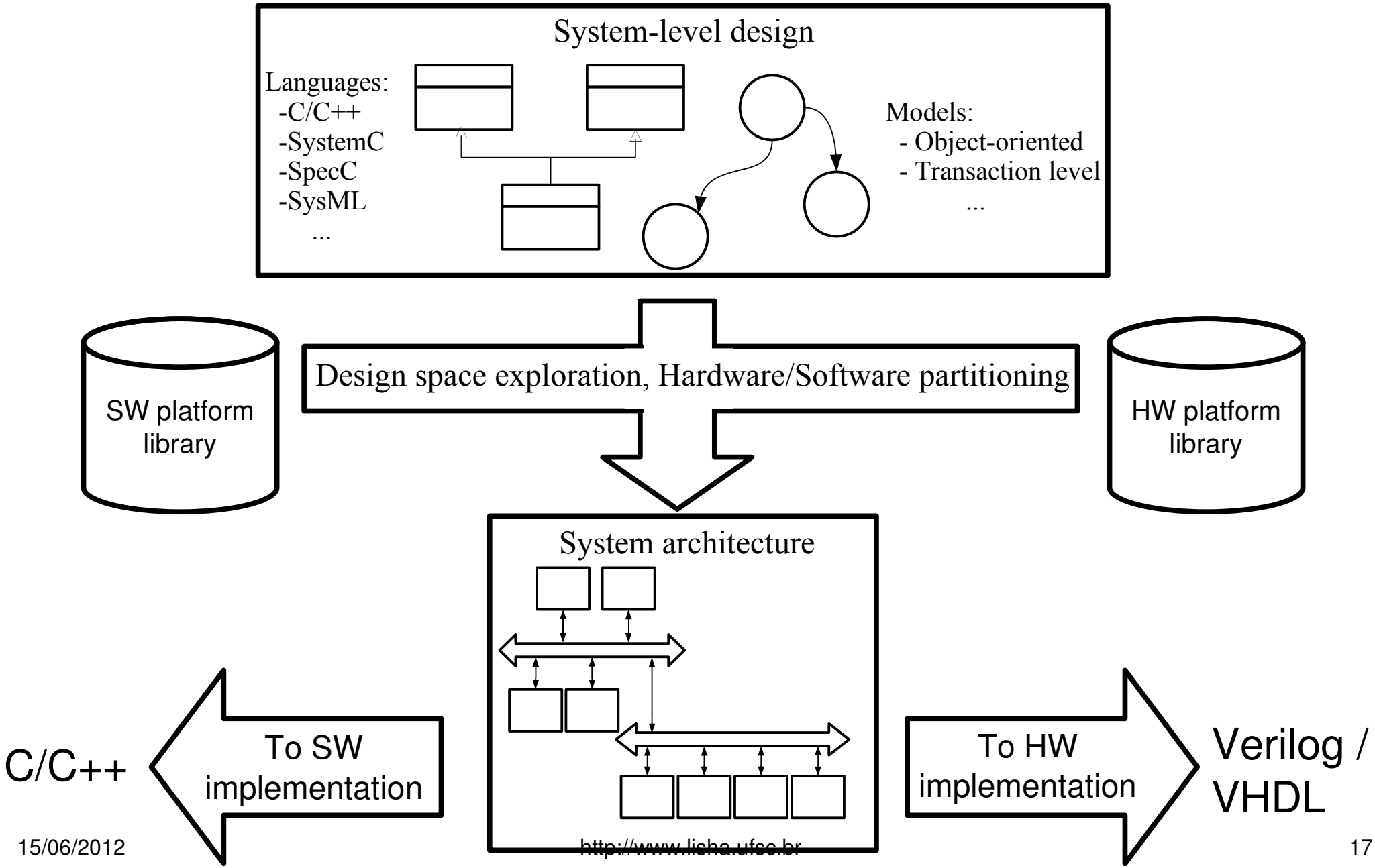
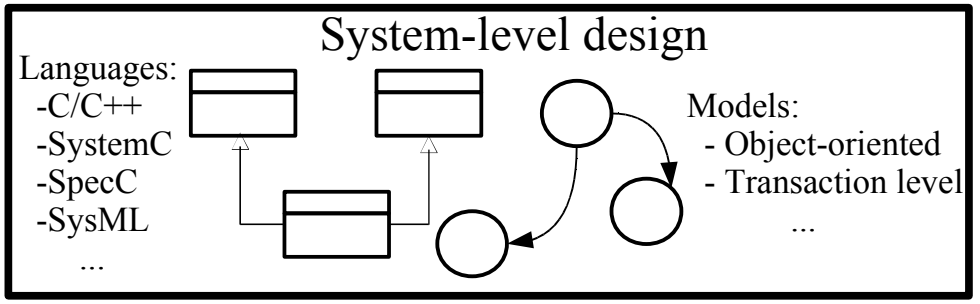


# Tomorrow's System-level design flow



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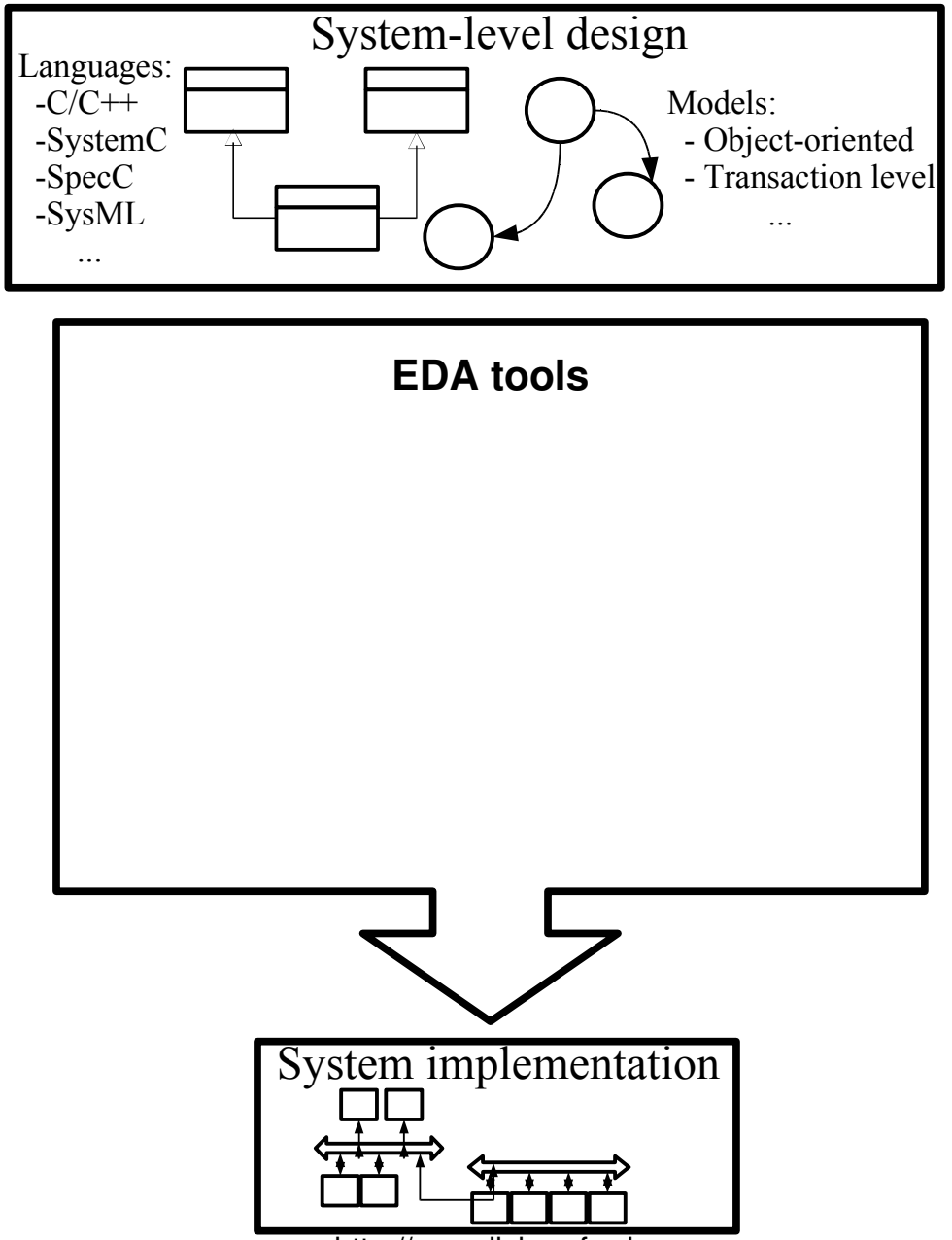

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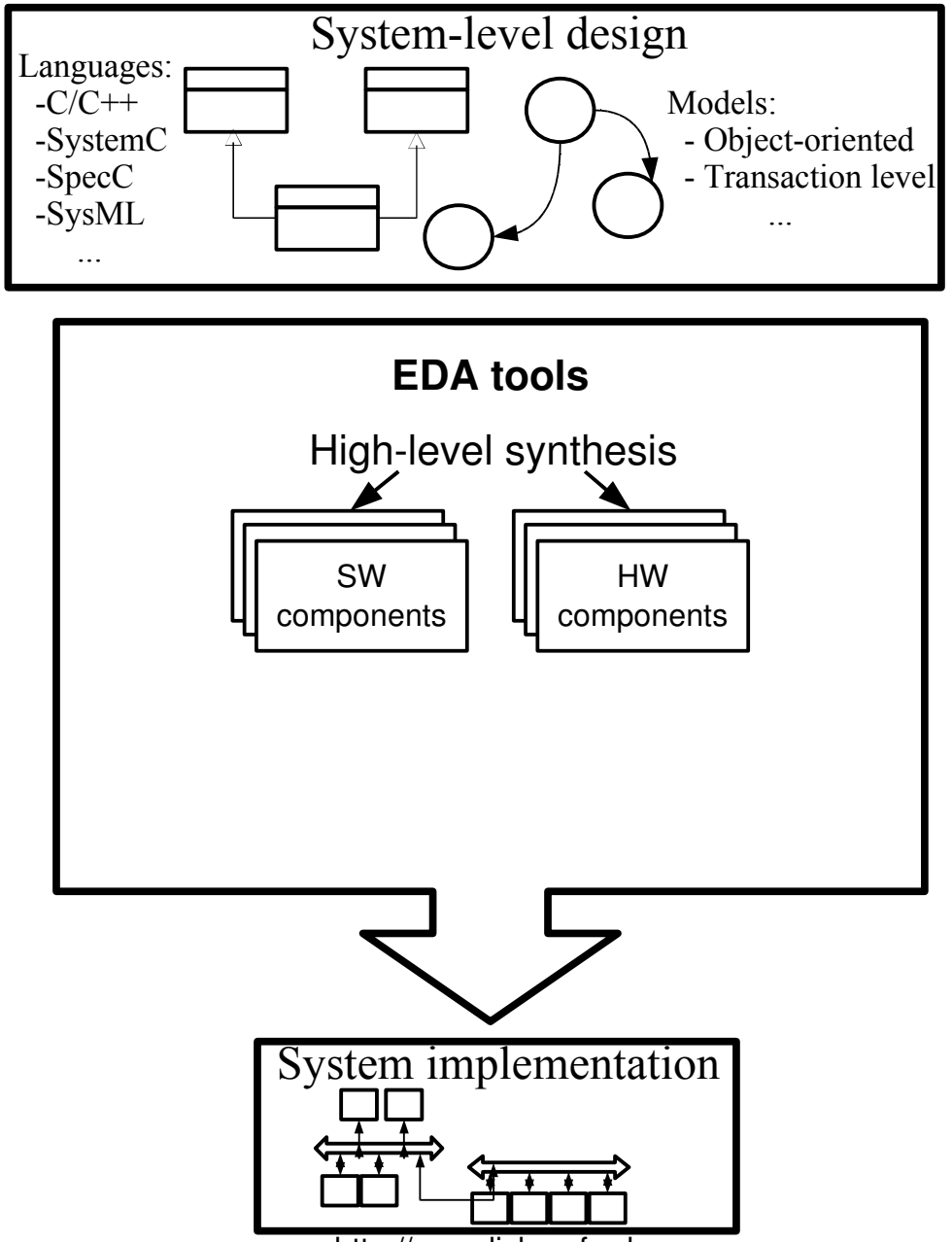

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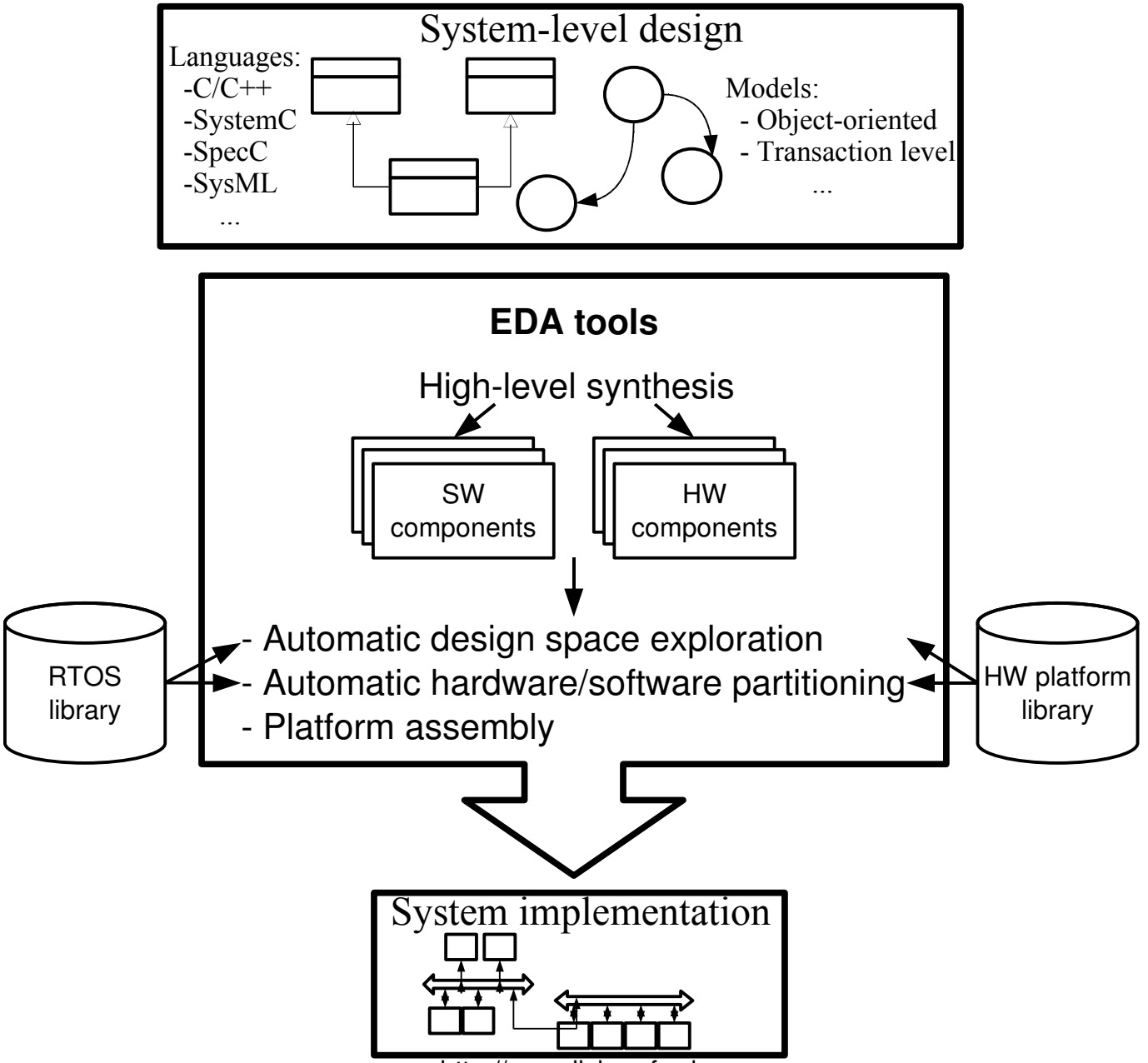

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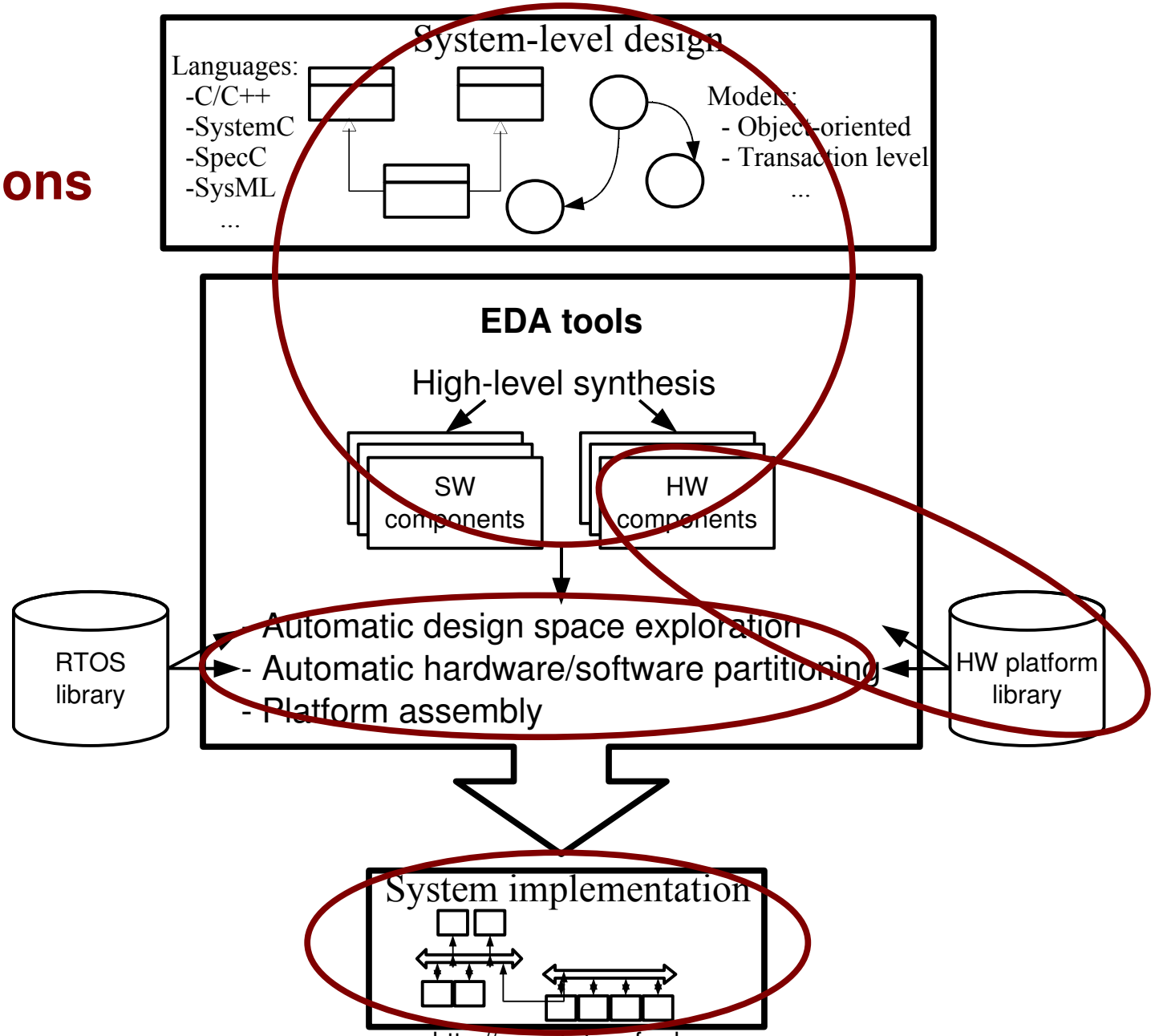
## Our Contributions



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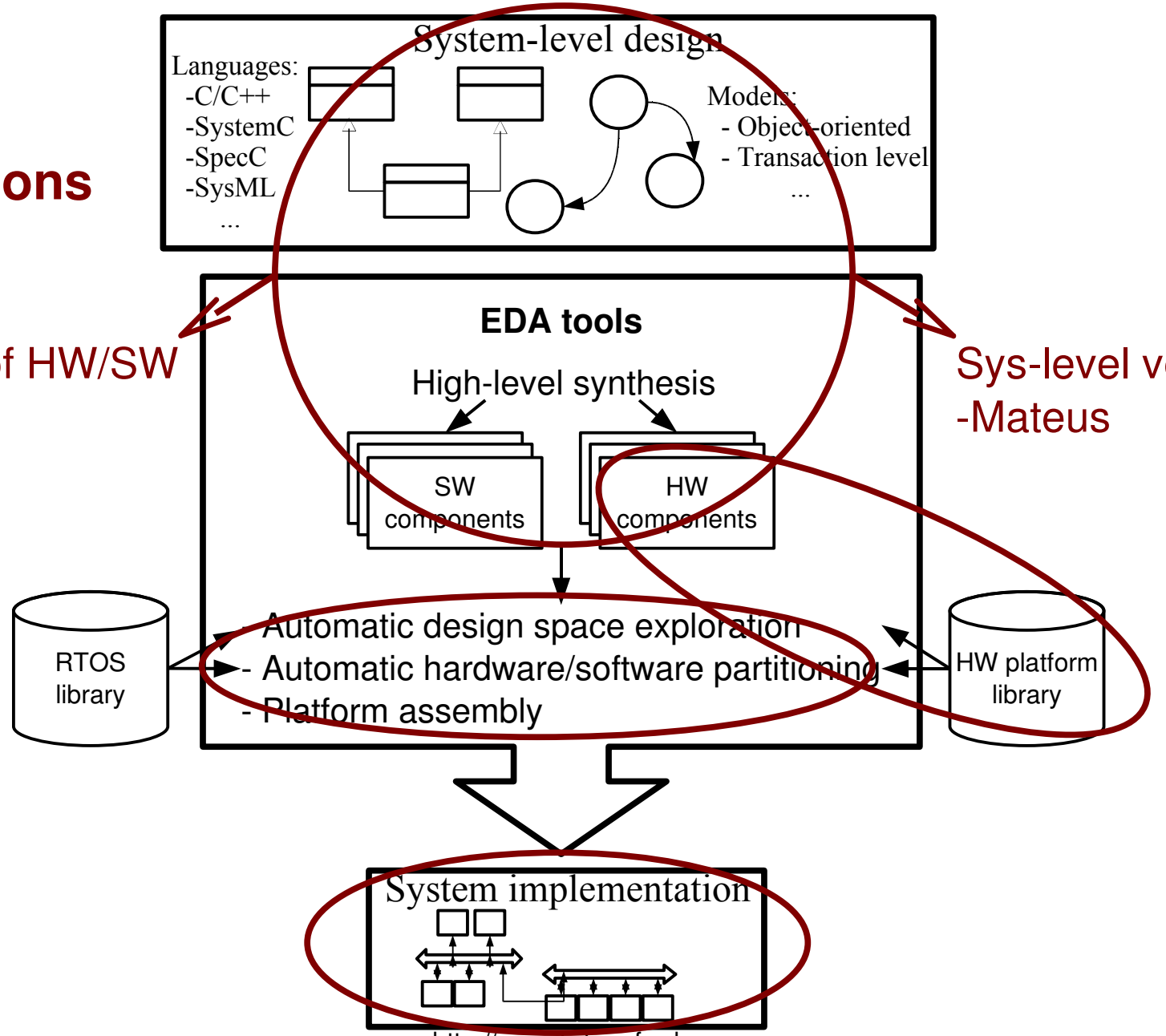


Unif. design of HW/SW
-Tiago

Sys-level verification
-Mateus

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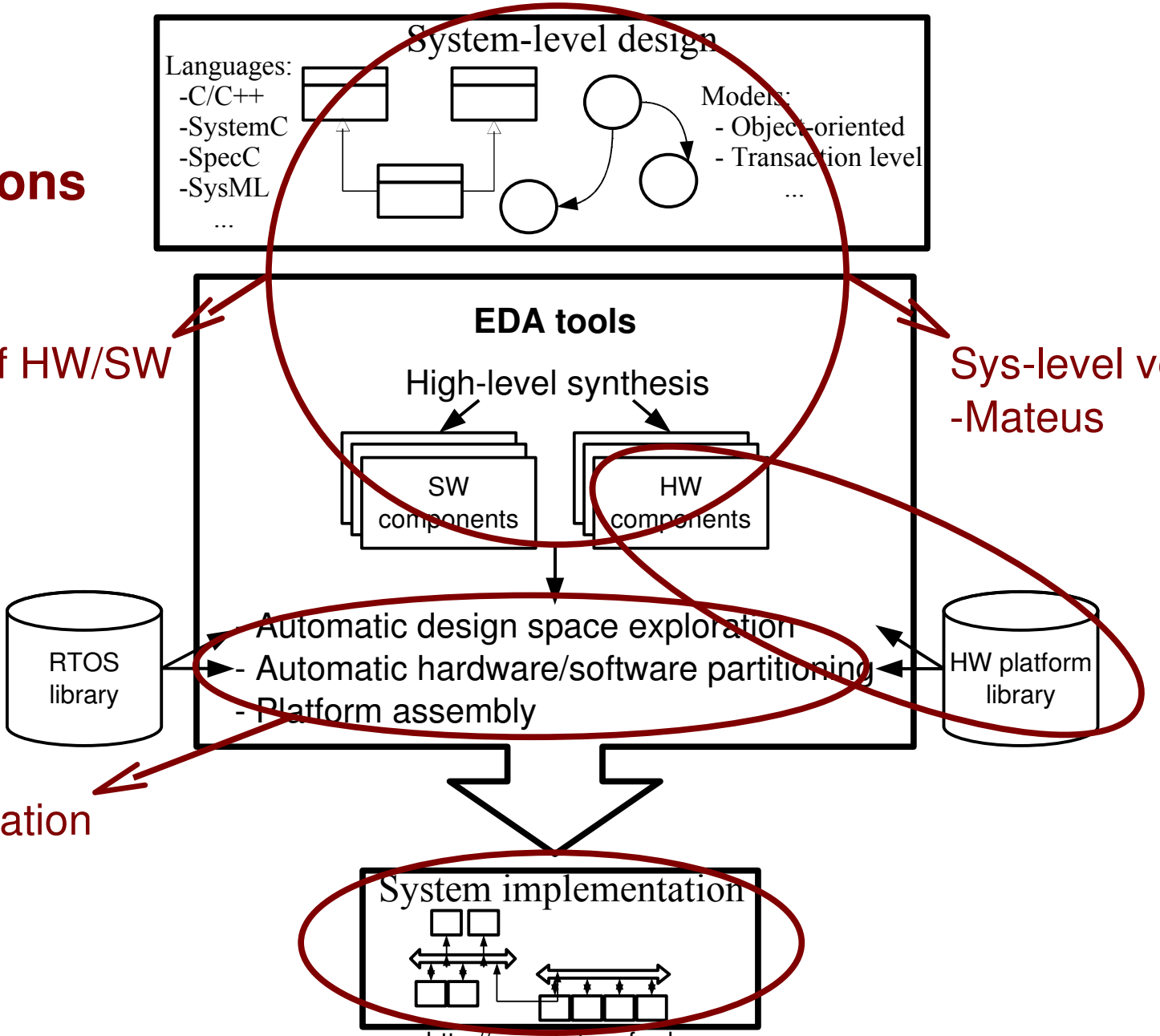
## Our Contributions

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ES generation
-Cancian

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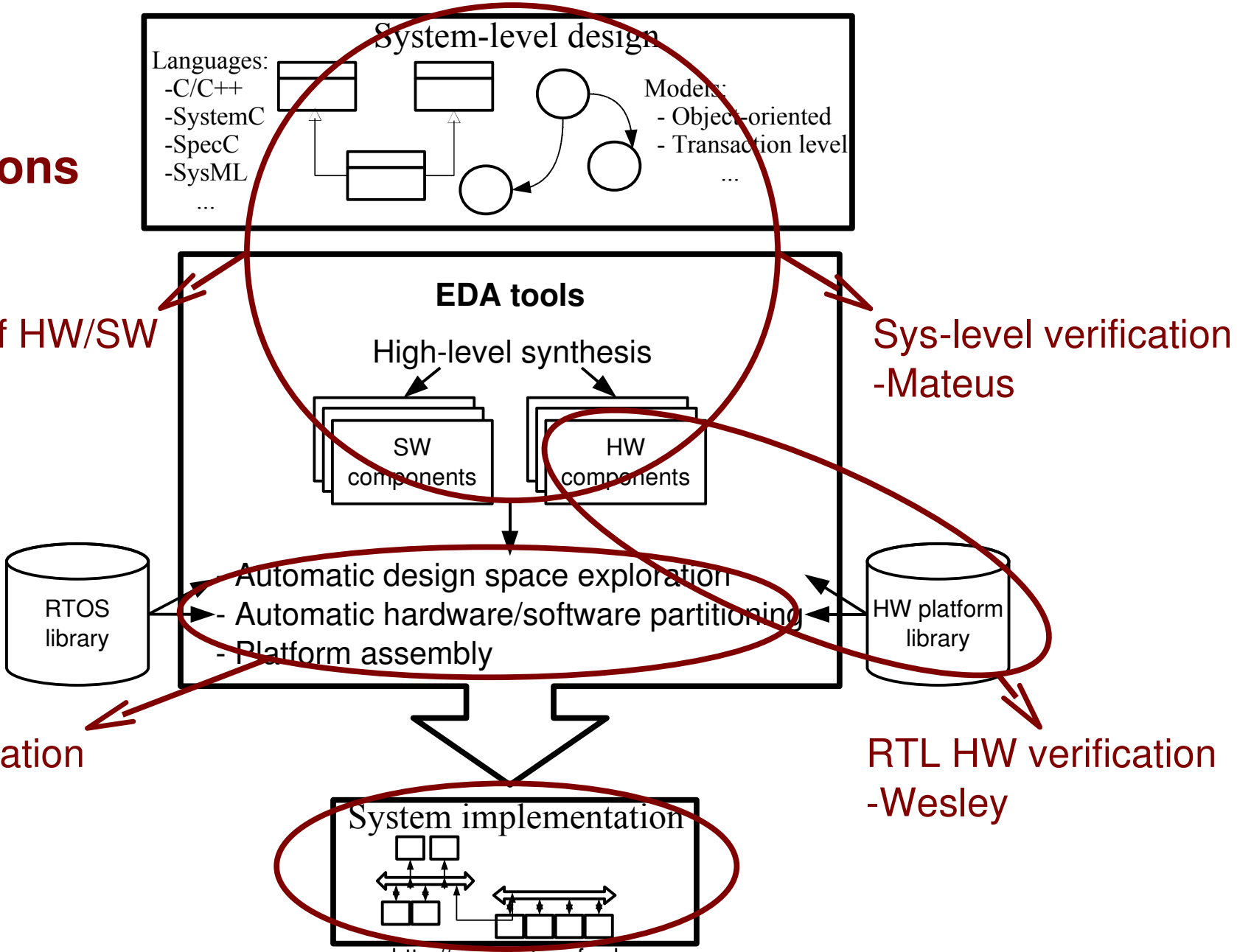

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